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Research Article

Design and Evaluation of an Optimized CMOS Layout for SRAM with Enhanced Power and Area Efficiency

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ABSTRACT

Various SRAM cell architectures, such as 10T, 9T, 8T, and 7T, are explored to enhance performance and stability, each offering improvements in specific regions while involving certain trade-offs. The number of transistors can be reduced to optimize area utilization by incorporating dynamic CMOS logic, which still enables the maintenance of high performance. In the present research, a novel sleepy technique combined with Adaptive Voltage Scaling (AVS) is proposed to design a low-power SRAM aimed at minimizing power consumption through the use of multi-threshold CMOS (MTCMOS) circuits. The proposed SRAM integrates sleep transistors with an additional leakage current feedback transistor in its MTCMOS-based structure, achieving effective results with respect to key parameters such as delay, power, and area.

Keywords: SRAM, Leakage, Sleepy Keeper Transistor, Dynamic Power, CMOS design, PMOS design.

I. INTRODUCTION

In earlier research, the primary design challenges for VLSI designers centered on device miniaturization and performance optimization. With the advent of deep sub-micron technology, high-performance integrated circuits have become feasible. Numerous studies have focused on designing and experimenting with portable devices intended for emerging applications such as space systems, wireless body-sensing networks, and medical implants. However, scaling down technology nodes has also resulted in increased static power dissipation. To address leakage power issues, various power reduction techniques have been proposed, including leakage feedback, stack keeper, body-biasing, and the sleepy keeper approach [2].

Furthermore, static RAM (SRAM) is widely utilized in embedded controllers, which demand minimal read and write access times. With the recent push toward lower operating voltages and reduced power consumption in memory systems, SRAM [8] has gained significant attention in research. On-chip memories, built using tightly packed SRAM cell arrays, enhance memory density and performance. A conventional 6T-SRAM [10] is commonly employed for these cells, where power dissipation primarily arises from two sources: static power and switching power. During active operation (ON-state), both static components of semiconductors and switching activity contribute significantly to power consumption. Conversely, during sleep or standby modes (OFF-state), leakage currents dominate power dissipation. With technology scaling, leakage power has become increasingly critical, often surpassing dynamic power in importance. Consequently, minimizing power dissipation has become a key concern for VLSI designers, particularly for battery-operated portable devices [1].

While designing the low-power VLSI circuit, the dissipation of power is considered as one of the challenging problems that is integrated with threshold voltage. Therefore, the minimization of threshold voltage maximizes the sub-threshold current leakage with the leakage power-dissipation enhancement that plays a significant part in total dissipation of power. Because of the leakage power problem, certain devices that are executed by battery for a long period in the mode of standby that are drained-out fast. To reduce the issues on SRAM was developed with dual-control-stacked-inverter that exploits dual-control-signals [6].

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The current research mainly focused on a novel sleepy stack technique with adaptive voltage scaling -AVS design development for low-power SRAM [9], [10] for minimizing power consumption utilizing multi-threshold CMOS circuit. The main contribution of the current research as follows: Section 2 explains the existing researches on low-power SRAM with the certain factors analyze and work process on different design metrics. Section 3 defines the proposed method for low power SRAM for reducing power-consumption using multi-threshold CMOS circuit. Section 5 explains the results and analysis with the power optimization methodologies and parameters. Finally, Section 6 explains the conclusion of the paper.

II. LITERATURE REVIEW

In **[3]**, the study explored an advanced **SEHF11T SRAM cell** architecture (comprising 11 transistors), specifically engineered to enhance **read static noise margin (RSNM)** and **write static noise margin (WSNM)** under aggressive technology scaling. This design effectively mitigates **write half-select disturbance** by incorporating a **cross-point data-aware write-word-line scheme**, which strategically reduces the vulnerability to **bit-interleaving** effects. Consequently, the proposed method enhances **soft-error immunity** and mitigates **multiple-bit upset (MBU)** occurrences in radiation-prone environments. Additionally, the architecture was rigorously evaluated across **process, voltage, and temperature (PVT) variations**, ensuring robust operation under corner conditions. A key feature of this approach is the **WSNM boost**achieved by temporarily disabling the feedback of **cross-coupled inverters** during the write cycle, known as the **power-cutoff write-assist technique**. However, it was observed that the comparative **SEWA10T cell** introduced increased **read access latency** due to the implementation of a **decoupled read buffer** employing three **series-connected transistors**, which trades off speed for noise isolation.

In **[4]**, the research introduced the **KLECTOR (Keeper-in-Leakage-Control Transistor) technique**, a novel leakage mitigation strategy for **standby-mode SRAM cells**. This method focuses on suppressing **subthreshold leakage currents**that dominate at reduced supply voltages and in deeply scaled CMOS nodes. The **KLECTOR circuit** minimizes power overhead by leveraging **self-controlled keeper transistors** positioned at the output node to regulate leakage paths without impacting active-mode performance. Simulation results demonstrated a substantial reduction in **static leakage power** — approximately **63% during write operations** and **69% during read operations** — when benchmarked against conventional SRAM designs. These analyses were performed using **Cadence EDA tools**, specifically the **Virtuoso analog design environment**, validating the efficacy of the proposed scheme under realistic design flows.

In **[5]**, the study primarily investigated **ultra-low-voltage SRAM architectures** aimed at achieving **minimum leakage power dissipation** without compromising data stability or access speed. The design utilized a **16×16 SRAM array**, incorporating optimized **column decoders, address circuitry, and sense amplifiers** to evaluate system-level efficiency. Comprehensive power analysis revealed that the proposed cell achieved **47.81% and 53.63% reductions in leakage power** under different operational scenarios, all while maintaining robust performance metrics. This work highlights the critical importance of addressing **standby leakage** and **dynamic switching power** concurrently, particularly for **battery-operated and IoT-oriented systems** where energy efficiency is paramount.

In **[7]**, a modified **9T-SRAM cell** architecture was proposed to outperform the traditional **6T-SRAM cell** by offering enhanced stability and reduced power-delay-product (PDP). The design was evaluated within a **4×4 SRAM array**, where comparative analysis demonstrated a **62.83% reduction in power consumption** at an operating frequency of **2 GHz**, alongside a **62.27% improvement in PDP** at the single-bit cell level. The implementation incorporated a **forced-sleep technique**, combining the benefits of **sleep transistor gating** and **forced stack effects** to achieve aggressive leakage suppression. Unlike conventional sleep methods where **PMOS transistors are gated with VDD** and **NMOS with GND**, the forced-sleep approach reverses these connections, yielding superior leakage control during idle periods. This methodology is particularly effective in **high-frequency, low-voltage environments**, making it suitable for next-generation **low-power cache memories** and **embedded SRAM arrays**.

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III. PROPOSED METHODOLOGY

The present research introduces a **novel sleepy technique integrated with Adaptive Voltage Scaling (AVS)** to achieve **ultra-low power SRAM operation**. This approach leverages **multi-threshold CMOS (MTCMOS) technology** to significantly reduce both **dynamic and static power dissipation** without degrading performance. The proposed SRAM cell employs **sleep transistors** in conjunction with an **additional leakage-current feedback transistor (LCFT)**, enabling improved control over leakage paths during standby mode. By incorporating the **MTCMOS primary structure**, the design effectively optimizes critical performance parameters such as **propagation delay, silicon area, and overall power consumption**. The **dynamic and static power components** — which traditionally escalate due to sleep-transistor-induced delay — are substantially mitigated through the **feedback-assisted leakage control mechanism**. Furthermore, **power optimization techniques** embedded within the architecture reduce overall energy consumption, thereby **lowering packaging costs** and **extending battery lifetime**, which is particularly vital for **portable and embedded memory systems**. The proposed design also achieves a **compact physical layout** by optimizing the **CMOS cell structure**, ultimately reducing area overhead compared to conventional approaches, while preserving stability and noise immunity across **PVT variations**.

3.1 Conventional SRAM:

The **conventional 6T-SRAM cell** employed in this research is designed to store a single **binary bit (logic '0' or '1')**using a **bi-stable latch circuit** [12]. The memory cell consists of two **cross-coupled CMOS inverters** forming a bistable structure that maintains data integrity in two stable states. To enable **read and write operations**, two additional **NMOS pass transistors (commonly referred to as access transistors)** are connected between the storage nodes and the complementary bit-lines (**BL** and **BLB**). These access transistors are controlled by the **word line (WL)** signal, which serves as the gate control for both read and write modes.

During a **write operation**, the WL is asserted high, turning ON the access transistors, thereby allowing data on the bit-lines to overwrite the stored value in the cross-coupled inverters. In contrast, during a **read operation**, the stored data is sensed via the voltage difference on BL and BLB, without disturbing the internal latch. When the WL is deasserted (low), the access transistors are switched OFF, effectively isolating the storage nodes from the bit-lines and placing the cell in **standby mode**, where the stored value remains unchanged.

This conventional **6T cell** forms the baseline architecture for comparative analysis against advanced designs (e.g., 9T, 10T, 11T variants) in terms of **power dissipation, noise margin, and read/write stability**. **Figure 1** illustrates the schematic of the conventional SRAM cell, while **Figure 2** presents the corresponding transient waveforms during typical read/write cycles, highlighting its operational phases.

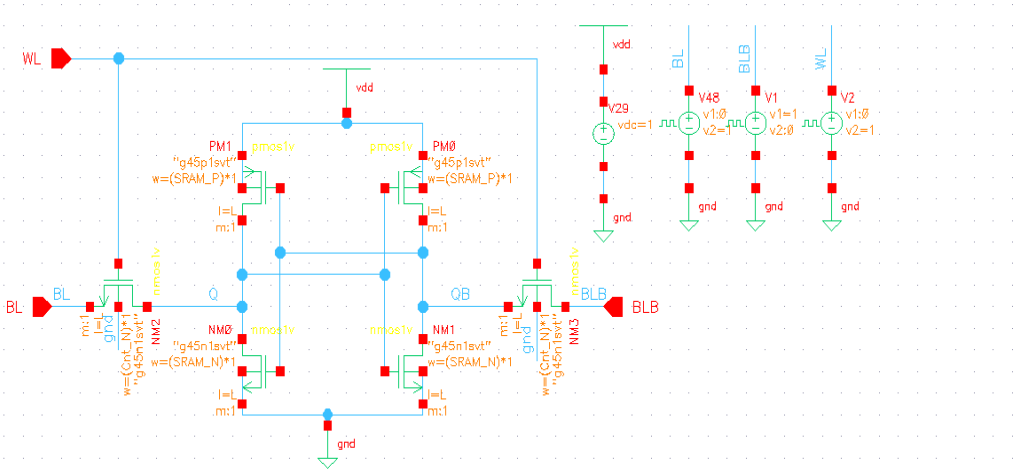

Figure 1 - Conventional SRAM

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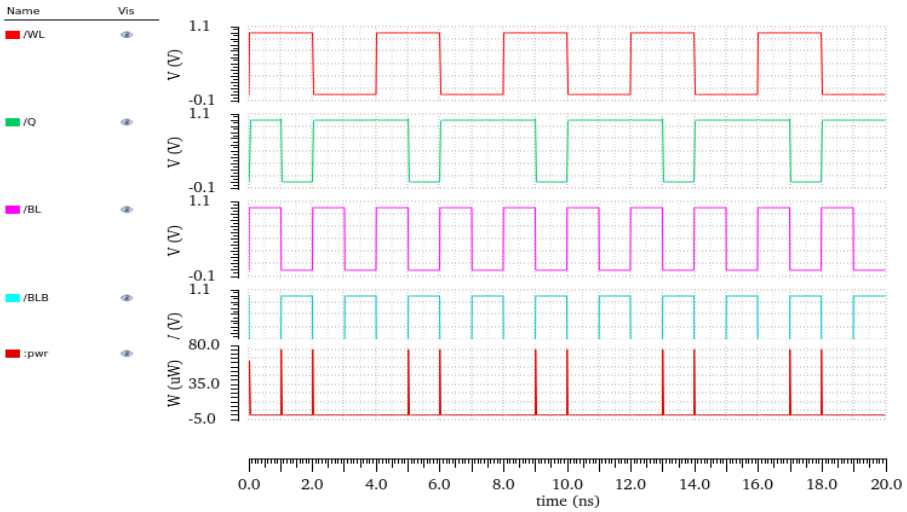

Figure 2 - Transient Waveform

3.2 Sleepy SRAM:

The sleepy SRAM executed with the circuit level methods that are performed earlier for minimizing sub-threshold-leakage-power method, which is a sleepy method. Therefore, the technology on sleepy SRAM utilizes sleep transistors in two places which has different phases. The pull-up network presented amidst Vdd (ST_P) and pull-down network presented amidst (ST_N) and Gnd. Here, the size of sleep transistor is provided, which is relative to either pull-down or pull-up transistor interconnected to the sleep transistor and the sleepy SRAM represented in Fig 3.

3.2.1 Active Mode

In the active mode state, the sleep signal represented as slp indicates the logic 1 with complementary sleep signal represented as slpb and voltage level, represented logic 0 with voltage level. Further, the sleep transistors (ST_P, ST_N) represented in active mode are ON. In the execution, when the power provided to the circuit with the sleep transistors turned ON with the outcome node on VP defined at VDD with the VG node presented at ground potential.

3.2.2 Sleep Mode

In the execution of sleep mode with the sleep signal represented as slp denoted with logic-0 with complementary sleep signal and voltage level slpb that defined the logic-1 voltage level. The sleep transistor denoted as ST_N and ST_P which are on the OFF state. Because of this reason, the ground and supply are isolated from the logic-circuit. Eventually, the static-power is set as virtually 0. Because of the effect on stack, the off-resistance increased with the minimization of leakage current. The technique generates state destruction with the floating voltage output, however, the outcome procured with the floating values after sleep mode. Addition of sleep transistors enhances the delay as well as area. In case of WL - word line raises high, the control-access transistors are in the position of ON condition, especially in the writing operation. Therefore, there are two complementary bit-lines that includes BL and BLB are interconnected to the cell, and the data obtained are written in the proper cell memory. In certain stage, SRAM cell is inaccessible from bit lines, while it was in standby mode. Here, the stored value sustains in unchanged position with the suppressed leakage current. These functioning are represented in Figure 3.

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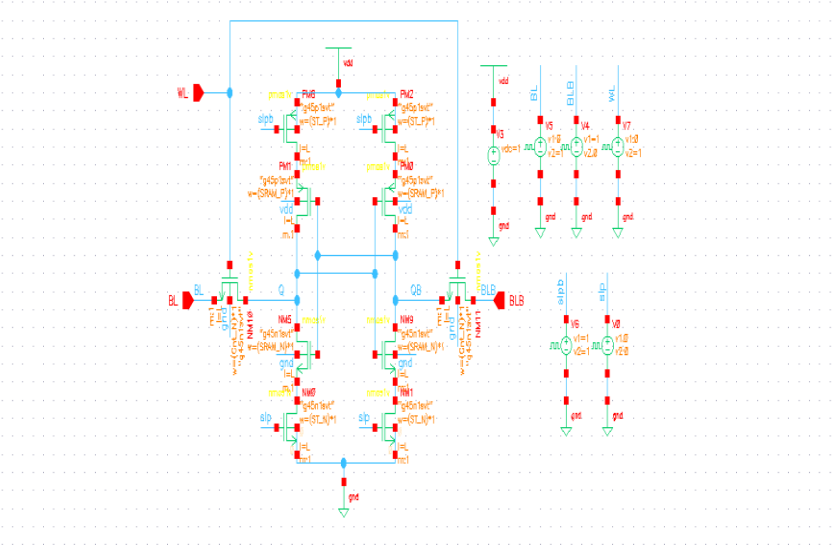

Figure 3 - Sleepy SRAM

3.3 Stack SRAM:

The stack method has been utilized in the research, which is considered as the another low-power-reduction strategy. Normally, it segregates the present transistor into 2-pieces and the transistors which was duplicated enable little reverse bias amidst the source and gate during the 2 transistors was in the OFF position (turned off) simultaneously. Because of the sub-threshold present dependency processed on gate bias with enhanced area and delay, obtained with a significant current minimization. Probably, certain execution resolves sleep method's limits with the help of maintaining state, however it enhances wake-up time. Eventually, the SRAM logic state circuit is also can be retained. Figure 4 represents the Stack SRAM Inverter.

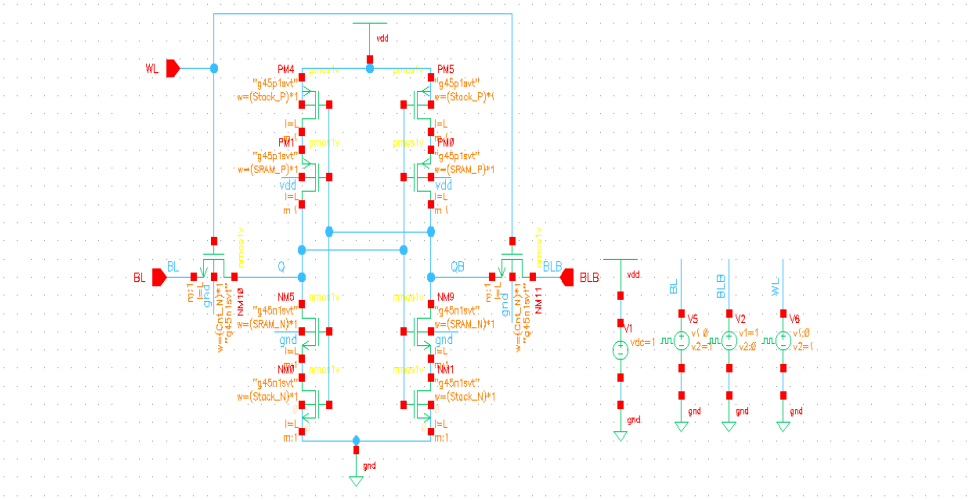

Figure 4 - Stack SRAM Inverter

3.3.1 Sleepy Keeper SRAM

This approach holds the sleepy method circuits maintain similar and in-addition with the P_MOS that defined as ST_P_K and N_MOS that defined as P_MOS transistors, that are combined in parallel amidst vdd, pull-down and pull-up network with gnd. Therefore, the effective way to utilize the CMOS transistors and PMOS, that are interconnected to NMOS and Vdd connection to gnd. At the same time, the NMOS transistors in the process are widely known for becoming ineffective at shifting Vdd and the PMOs-transistors are widely known for becoming inefficient at shifting Gnd. Certain floating voltage output has been surmount with the introduction of sleepy-keeper

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method. In case of sleep-mode, the ST_P sleepy PMOS-transistors has to be turned OFF with the N_MOS transistors (ST_N_K) interconnected amidst oull-up n/w and VDD that holds specific data that represented as “1”, which is turned “ON”. Likewise, in order to turn “ON” the P_MOS-transistor with the data holding ‘o’, that are interconnected amidst the GND and pull-down N/W with the ST_N sleepy NMOS-transistor to turn in the state “OFF”. Hence, this enables to keep the specific data utilized in the process are safe, especially in sleep or standby mode. During the WL drives high with the turned “ON” position of control- access transistors in writing operation. The 2-complementary bit-lines such as BL and BLB in writing operation are interconnected to the cell with the written message on data in memory cell. In certain cases, SRAM cell is unobtainable from bit lines after the SRAM denoted in standby-mode, in the certain cases, the stored data keeps unchanged. Figure 5 & 6 represents the Sleepy Keeper SRAM and transient waveform of it.

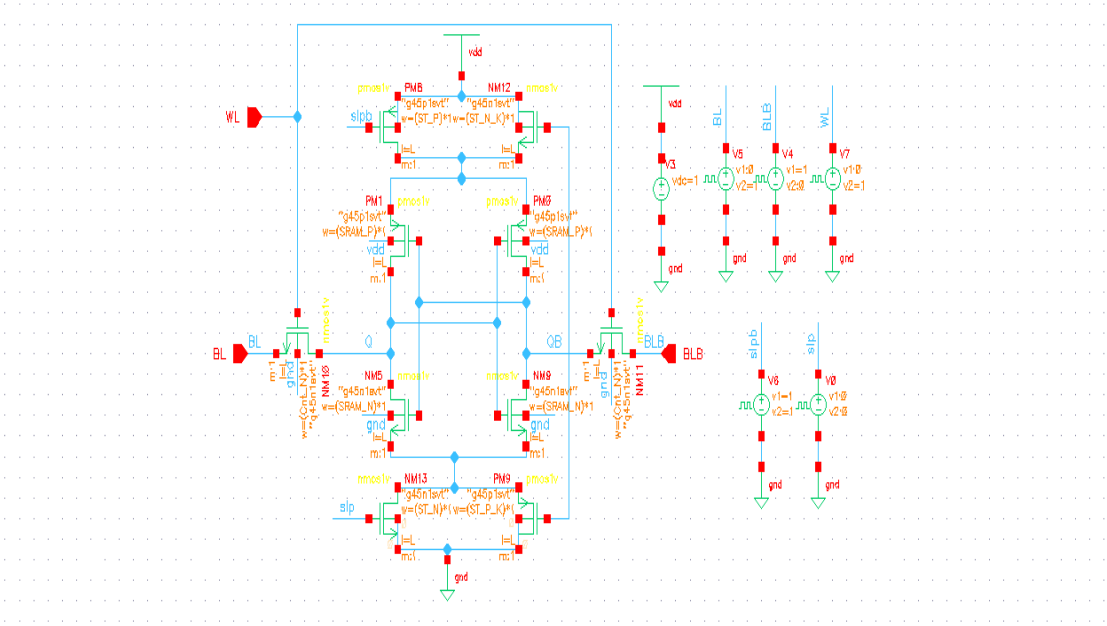

Figure 5 - Sleepy Keeper SRAM

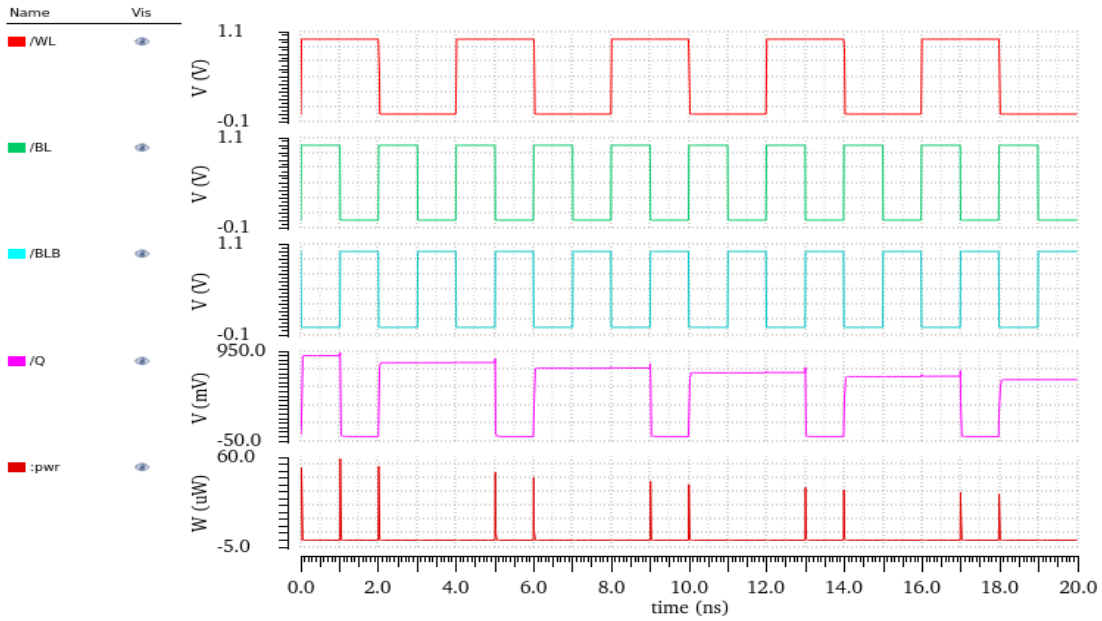

Figure 6 - Transient Waveform for sleepy Keeper SRAM

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3.4 LECTOR SRAM

The main theme of using this method is to enhance the transistor number in the "OFF" state in the gnd path and source. Therefore, the 2-leakage control transistors that includes NMOS (LCT_N) and PMOS (LCT_P) interconnected amidst pull-down and pull-up network. The PMOS gate terminal is interconnected to empty the SRAM_N pull-down network, which is interconnected to empty the SRAM_P pull-up network. The PMOS body terminal is interconnected to Vdd and NMOS is interconnected to gnd. In the process of sleep-mode, the selection of NMOS transistor or PMOS transistors(any one) should be in the "OFF" state or close to cut-off area. Normally, this raises the path in resistance amidst gnd and Vdd and this method, also minimized the leakage power. Hence, the LCT-transistor size is optimized in the research for effective outcome and the enhancement of dynamic power with the SRAM static-power is minimized.

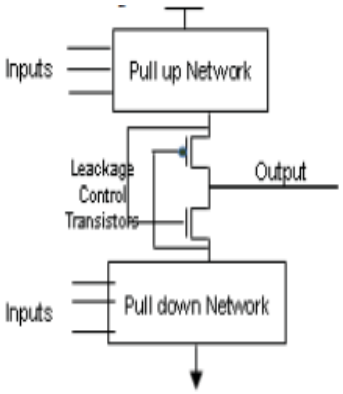

Figure 7 - Process of LECTOR SRAM

During the WL drives high with the turned "ON" position of control- access transistors in writing operation. The 2-complementary bit-lines such as BL and BLB in writing operation are interconnected to the cell with the written message on data in memory cell. In certain cases, SRAM cell is unobtainable from bit lines after the SRAM denoted in standby-mode, in the certain cases, the stored data keeps unchanged. Figure 7 indicates the process of LECTOR SRAM and Figure 8 & 9 represents the LECTOR SRAM and transient waveform of it.

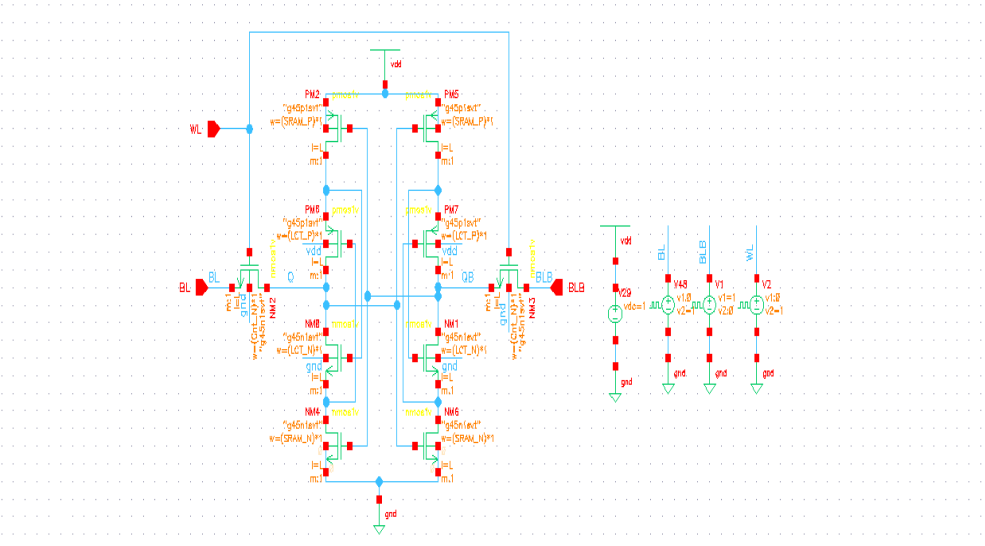

Figure 8 - LECTOR SRAM

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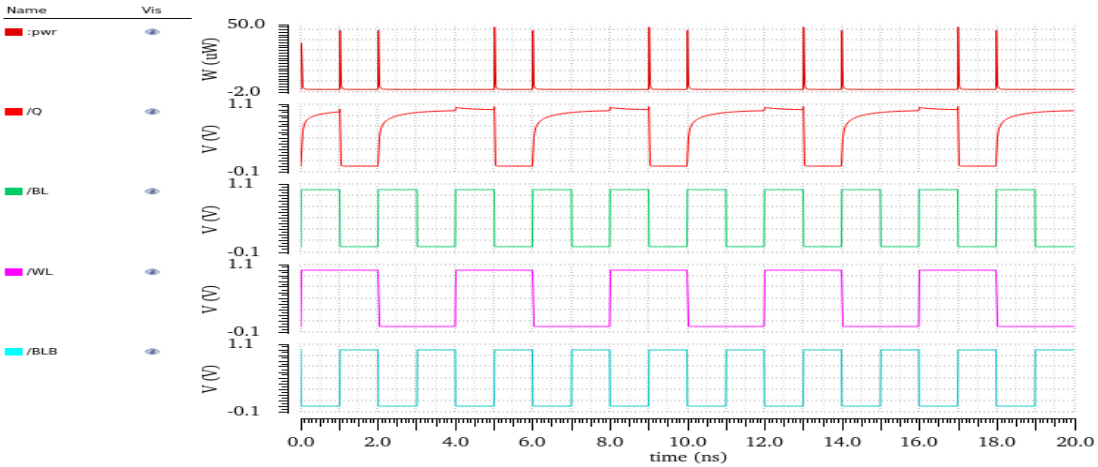

Figure 9 - Transient Waveform for LECTOR SRAM

3.4.1 Sleepy Keeper LECTOR SRAM

This method are processed with a combination of LECTOR and sleepy keeper method. During the process of sleep mode with the sleepy transistor represented as ST_P and ST_N, which are turned OFF. Therefore, the parallel transistors includes ST_P_K and ST_N_K that helps in holding the data in sleep-mode that reduces the leakage power and the power minimization done by LCT_N and LCT_P due to the multiple transistors in sleep mode and "OFF" state that enhances the resistance path amidst gnd and vdd. During the WL drives high with the turned "ON" position of control- access transistors in writing operation. The 2-complementary bit-lines such as BL and BLB in writing operation are interconnected to the cell with the written message on data in memory cell. In certain cases, SRAM cell is unobtainable from bit lines after the SRAM denoted in standby-mode, in the certain cases, the stored data keeps unchanged. Figure 10 & 11 represents the Sleepy Keeper LECTOR SRAM and transient waveform of it.

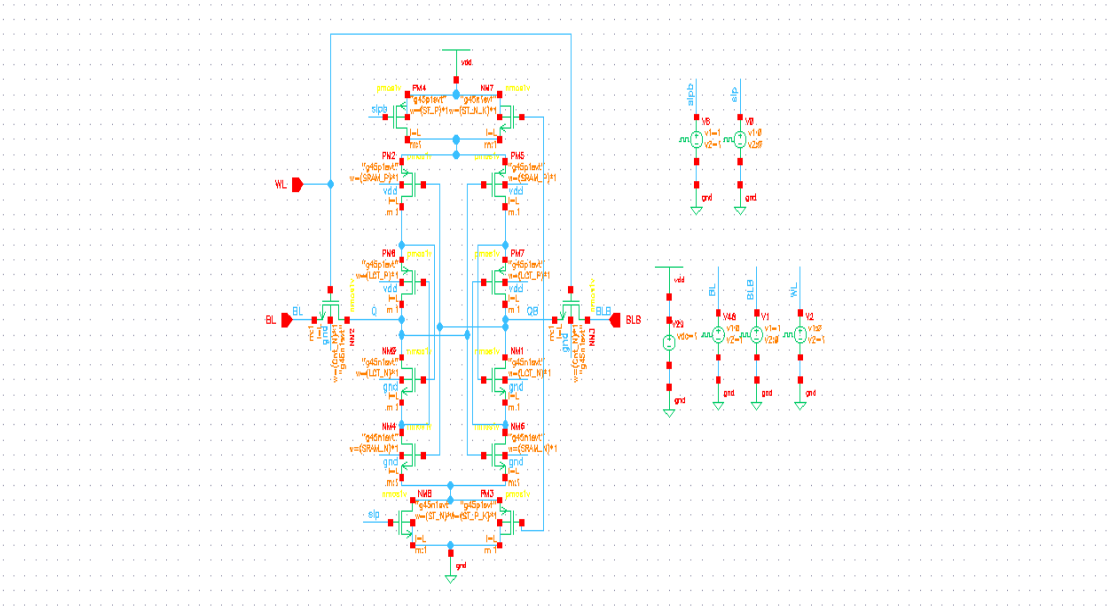

Figure 10 - Sleepy Keeper LECTOR SRAM

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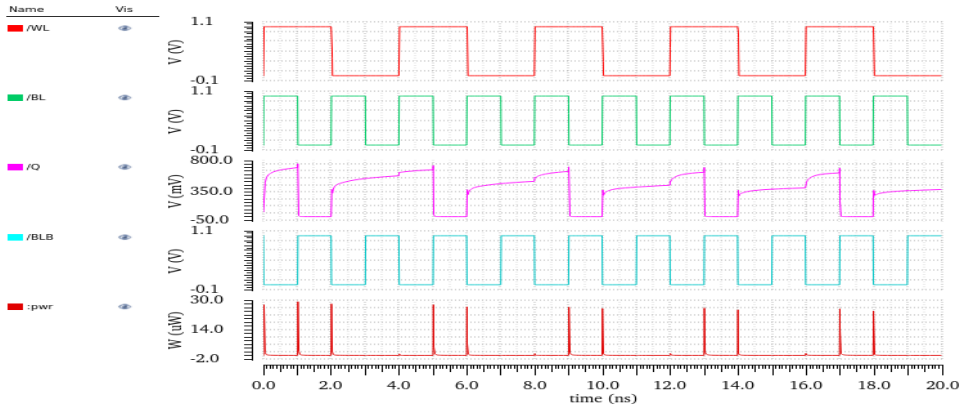

Figure 11 - Transient Waveform for Sleepy Keeper LECTOR SRAM

3.4.2 Sleepy Stack SRAM

The sleepy stack SRAM [11] structure used in the research defines a novel technique that minimizes leakage power with the integration of the sleep and stack transistor structure. Here, the sleep stack method has 2-modes that define as first and second mode in sleep condition. By using a forced stack method in the research, the previous transistors used are split into 2-transistors with the benefits of stack structure from the effect of stack. On the other hand, sleep transistors are placed parallel to a transistor (stacked) to achieve state retention and low-power leakage by integrating these techniques.

3.4.2.1 Active Mode

In the Active Mode, the sleep transistors are in "ON" state of the sleepy-stack transistor. Therefore, this mode have the possibility to allow for circuit delay minimization and all the presented sleep transistors are in "ON" state, in the mode of active that outcomes in a rapid switching time. During the process of transistor, which is parallel to sleep-transistors, the voltage of threshold value may be attained to high.

3.4.2.2 Sleep Mode

In the sleep-mode, the transistors are disabled with the preservation of precise logic state using the structure of sleepy stack. It is noted that the sleep transistors are being in a state of "OFF" that results in the effect of stack, that minimizes leakage power consumption. Utilizing the sleep stack method enhances the speed in different ways during the sleep transistor on the state of "ON", and current flows via the circuit. Hence, it is significant to switch circuit speed and it is enhanced with the minimized delay.

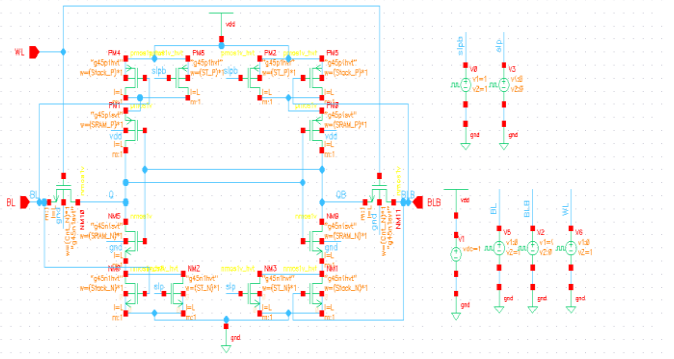

Figure 12 - SRAM block using Sleepy Stack Technique

3.5 SNM (Static Noise Margin)

The memory cell stability has been acquired in the noise presence is evaluating utilizing static noise margin. Therefore, it can be featured with the lowest-voltage that should be enabled to store nodes for a certain state to flip.

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There is a possibility to measure SNM by including the voltage transfer features of the 2-inverters that imparted in the memory cell. Further, the inverters of memory cell's are developed to manage stable states with the output nodes includes the data that is stored in the memory. Further, the node voltages initialized varying due to the noise presented at the storage nodes that results in a cell stability decline of 55. The utilization of SNM evaluates the maximum permit level of noise voltage with the capability of these inverters management with their current state in the noise presence.

Moreover, employed an advanced low-power processors with DVS - dynamic-voltage-scaling, which is considered as a feasible option, especially for power reduction. With the help of the DVS, the operation of system is executed in the highest frequency at the specific supply VDD and VDDnom that defines nominal supply-voltage. Therefore, it can be operated in low power-mode at the scaled-VDD. The significant utilization of supply voltage, which is minimized than its value at nominal stage in the scheduled tasks completion with the minimum energy usage amount.

In the modern digital VLSI-systems [14] along with the utilization of SRAM cells that share a substantial portion, that have the similar supply-voltage with the other processing units. Therefore, since the another digital components that are executed at their lowest energy-point with the continuation of SRAM that operates with reliability at specific scaled VDD. The different stages such as M1, M2, M3, M4, M5, M6, and M7 that defines Conventional Technique, Sleepy SRAM, Stack SRAM, Sleepy Keeper Technique, LECTOR technique, SK-LCT technique [13], and Sleepy Stack SRAM.

IV. RESULTS AND DISCUSSION

The current research focused on a novel sleepy technique along with AVS design is proposed for low-power SRAM for reducing power consumption utilizing multi-threshold CMOS circuit. In the part of power dissipation, it has been analyzed with the PDP - Power-Delay-Product - PDP, Leakage-current, Energy-delay-product - EDP, and PEP - Power-Energy-Product, duty-cycle, and Clock Frequency. The layout of the developed schematic for existing design has been mentioned in the research previously. The parameter used in the research such as Area (µm), tpdf (ps), tpdr (ps), propagation delay tpd (ps), Static power (W), dynamic power NMOS (W), dynamic power PMOS (W), power (J), energy (J), PDP (J), PEP (J), EDP (J), clock frequency (Hz), and duty cycle (Q) on power optimization methodologies such as M1 (con), M2 (sleepy), M3 (stack), M4 (SK), M5(LEC), M6(SK_LEC), and M7 (SS-hvt transistor) represented in Table I. Here, in the current research, figure 13 represents the layout of the conbf, the conventional technique.

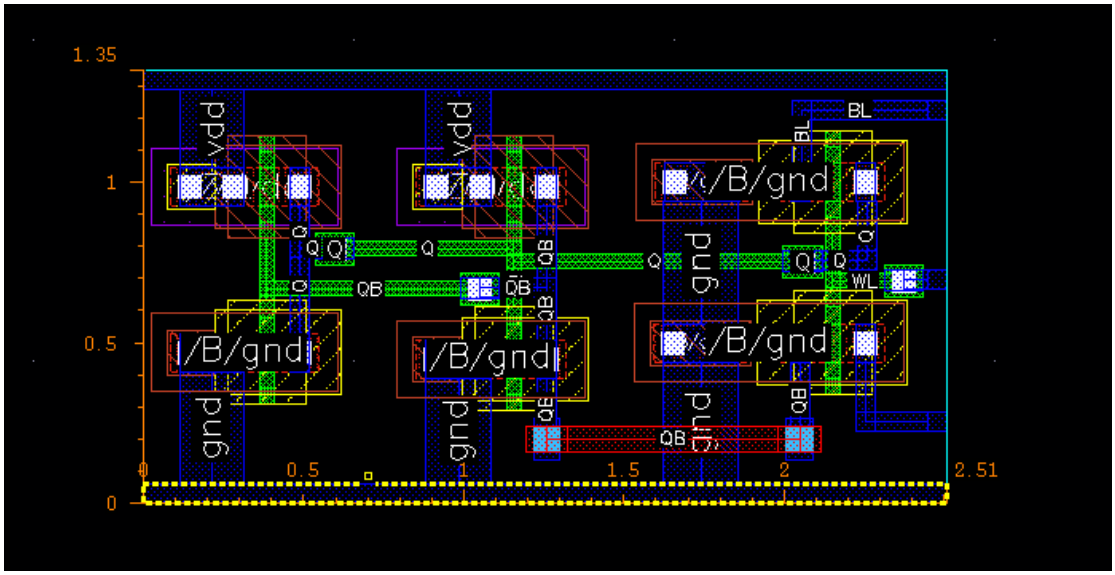

Figure 13 - Layout of the Conventional Techniques

The layout of the LEC, SK, SK_LCT, sleepy layout, sleepy stack, and stack has been denoted in the simulation process in figure 14 a, b, c, e, f, g, and h.

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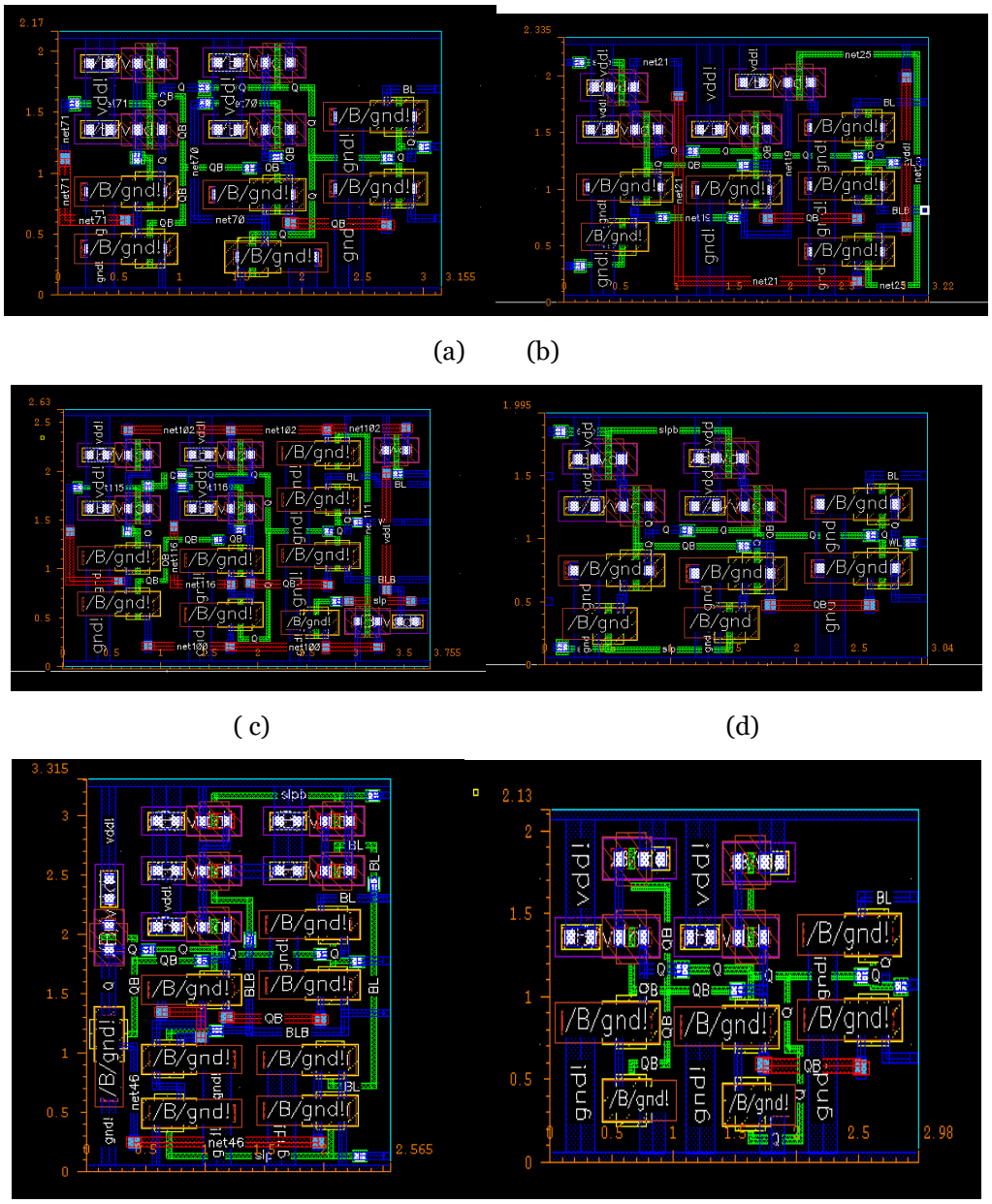

Figure 14 - (a) LEC (b) SK (c) SK_LCT (d) Sleepy layout (e) Sleepy Stack & (f) Stack

Table I - Comparison of proposed work with the Existing Researches with the Power Optimization Methodologies based on parameters

SL. No	Parameter	Power Optimization Methodologies						
		M1 (con)	M2(sleepy)	M3(stack)	M4(SK)	M5(LEC)	M6(SK_LEC)	M7 (SS-hvt transistor)
1	Area (µm)	3.3885	6.0648	6.3474	7.5187	6.8464	9.8757	8.502975
2	tpdf (ps)	10.882	5.874	7.454	5.536	5.642	4.436	5.833

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3	tpdr (ps)	28.306	26.660	28.264	29.796	29.979	49.648	11.228
4	Propagation Delay tpd (ps)	19.594	16.267	17.859	17.666	17.810	27.042	8.530
5	Static Power (W) Vin=0V	2.381E-6	76.148E-12	712.94E-12	43.481E-12	1.036E-6	42.503E-12	146.87E-12
6	Static Power (W) Vin=1V	1.427E-6	35.13E-12	421.81E-9	26.641E-12	5.633E-9	25.318E-12	9.154E-12
7	Dynamic Power (W) NMOS	13.559E-9	30.364E-12	2.417E-9	45.246E-12	459.26E-12	11.990E-12	40.709E-12
8	Dynamic Power (W) PMOS	133.29E-9	167.874E-12	29.047E-9	192.56E-12	47.855E-9	111.554E-12	206.854E-12
9	Power (W)	1.041E-6	363.603E-9	651.243E-9	363.378E-9	526.87E-9	220.169E-9	336.64E-9
10	Energy (J)	2.560E-15	601.591E-18	1.513E-15	450.56E-18	1.511E-15	445.682E-18	354.708E-18
11	PDP (J)	20.40E-18	5.914E-18	11.630E-18	6.419E-18	9.383E-18	5.953E-18	2.871E-18
12	PEP (J)	2.665E-21	218.741E-24	985.966E-24	163.72E-24	796.17E-24	98.125E-24	119.409E-24
13	EDP (J)	50.17E-27	9.786E-27	27.038E-27	7.959E-27	26.914E-27	12.052E-27	3.025E-27
14	Clock Frequency (Hz)	500M	500M	500M	500M	500M	500M	500M
15	Duty Cycle Q (%)	69.73	69.53	69.64	69.48	69.88	41.69	74.98

This research also compared with the parameters in the research such as Area (µm), tpdf (ps), tpdr (ps), propagation delay tpd (ps), Static power (W), dynamic power NMOS (W), dynamic power PMOS (W), power (J), energy (J), PDP (J), PEP (J), EDP (J), clock frequency (Hz), and duty cycle (Q) on power optimization methodologies such as M1 (con), M2 (sleepy), M3 (stack), M4 (SK), M5(LEC), M6(SK_LEC), compared with M7 (SS-hvt transistor) represented in Table II with increment and decrement values. The inc represents the proposed value increased compared to existing method and dec represents the proposed method value decreases compared to existing method.

4.2 Comparison table on Parameter with the value increment and value decrement on M1, M2, M3, M4, M5, and M6 with M7

SL. No	Parameter	M1 vs M7		M2 vs M7		M3 vs M7		M4 vs M7		M5 vs M7		M6 vs M7	
1	Area (µm)	60.15	inc	28.67	inc	25.35	inc	11.58	inc	19.48	inc	16.14	dec
2	tpdf (ps)	86.56	dec	0.70	dec	27.79	dec	5.09	inc	3.27	inc	23.95	inc
3	tpdr (ps)	60.33	dec	57.88	dec	60.27	dec	62.32	dec	62.55	dec	77.38	dec

4	Propagation Delay tpd (ps)	56.47	dec	47.56	dec	52.24	dec	51.72	dec	52.11	dec	68.46	dec
5	Static Power (W) Vin=0V	99.99	dec	48.15	inc	79.40	dec	70.39	inc	99.99	dec	71.06	inc
6	Static Power (W) Vin=1V	100	dec	73.94	dec	100.00	dec	65.64	dec	99.84	dec	63.84	dec
7	Power (W)	67.66	dec	7.42	dec	48.31	dec	7.94	dec	36.11	dec	52.90	inc

V. CONCLUSION

The current research emphasizes a **novel sleepy technique combined with Adaptive Voltage Scaling (AVS)** to achieve **low-power SRAM operation** through the use of **multi-threshold CMOS (MTCMOS) circuits**. In this work, a **high-speed, energy-efficient SRAM architecture** is developed and benchmarked against multiple low-power design methodologies, including the **Conventional 6T-SRAM**, **Sleepy SRAM**, **Stack SRAM**, **Sleepy Keeper Technique**, **LECTOR (Leakage Control Transistor) Technique**, **SK-LCT (Sleepy Keeper–Leakage Control Transistor) Technique**, and **Sleepy Stack SRAM**. This comparative framework allows for a detailed evaluation of trade-offs in **power, delay, and stability metrics** across different design approaches.

In modern **digital VLSI systems**, **SRAM arrays** occupy a substantial portion of the on-chip area and share the **same supply voltage (VDD)** with other processing units. As technology scales, these digital blocks are increasingly operated at their **minimum energy point (MEP)** to extend battery life and reduce thermal dissipation. However, maintaining **SRAM reliability** at scaled supply voltages is challenging due to degraded **read static noise margin (RSNM)**, **write-ability issues**, and heightened **leakage currents**. Thus, integrating **sleep-based power-gating** with **AVS control** enables dynamic voltage adaptation, ensuring **robust operation** of the SRAM cells while optimizing **energy efficiency** across various workload conditions.

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