Journal of Information Systems Engineering and Management
2024, 9(4s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

Resource-Optimized FIR Filter Architecture with Coefficient Reuse for ASIC Design

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ARTICLE INFO

Received: 17 June 2024

Revised: 21 Aug 2024

Accepted: 09 Oct 2024

ABSTRACT

This work presents the design, functional verification, and ASIC synthesis of a digital FIR filter architecture optimized through coefficient reuse. The proposed method exploits symmetry in filter coefficients to minimize redundant multiplications, thereby reducing hardware complexity without compromising accuracy. RTL implementation in Verilog was verified using simulation waveforms, confirming correct convolution behavior under varied input sequences. The design was synthesized using Cadence Genus with a 1.0 V standard cell library, achieving an area utilization of 1675 units across 482 cells. Power analysis reported a leakage of 96 nW and dynamic consumption of 26 µW, demonstrating efficiency suitable for low power signal processing applications. Timing analysis highlighted feasible propagation delays through arithmetic stages, validating the design's readiness for ASIC integration. The results establish coefficient reuse as a practical optimization strategy, delivering a compact, power efficient, and functionally robust FIR filter architecture for advanced signal processing systems.

Keywords: Digital FIR filter, coefficient reuse, Verilog RTL, functional verification, ASIC synthesis, low-power design, area optimization, timing analysis, signal processing architecture, Cadence Genus.

Introduction

Digital filters are indispensable components in modern signal processing systems, widely applied in communications, biomedical instrumentation, image enhancement, and audio processing. Among them, Finite Impulse Response (FIR) filters are preferred for their inherent stability and linear phase characteristics, making them suitable for high-precision applications [1], [2]. The design of FIR filters for hardware platforms such as FPGA and ASIC has been extensively studied, with emphasis on optimizing power, area, and throughput [3], [4]. Conventional FIR architectures, however, demand multiple multipliers and adders, which significantly increase silicon area and dynamic power consumption in ASIC realizations [5], [6].

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To address these challenges, researchers have explored architectural optimizations such as Distributed Arithmetic (DA), multiplier less designs, and coefficient symmetry exploitation [7], [8]. Coefficient reuse, in particular, leverages the symmetry of filter coefficients to reduce redundant multiplications, thereby lowering hardware complexity without compromising accuracy [9], [1]. This approach is especially beneficial in ASIC implementations, where resource efficiency directly translates into reduced silicon area and lower power dissipation [10], [6]. By combining coefficient reuse with optimized adder tree structures, FIR filters can achieve high throughput while maintaining compact design footprints.

Functional verification plays a critical role in validating such architectures before synthesis and layout. RTL simulation ensures correctness of convolution operations under varied input conditions, while synthesis reports provide quantitative insights into area, power, and timing behaviour [11], [6]. ASIC synthesis using Cadence Genus or Synopsys Design Compiler allows designers to evaluate leakage and dynamic power, cell utilization, and timing slack under realistic process, voltage, and temperature (PVT) conditions [2], [4]. These metrics are essential for demonstrating the practical viability of coefficient reuse in industrial signal processing systems.

This paper presents the ASIC implementation of a digital FIR filter optimized through coefficient reuse. The design was modelled in Verilog RTL, functionally verified using waveform simulations, and synthesized using Cadence Genus with a 1.0 V standard cell library. Results show significant reductions in area and dynamic power compared to conventional FIR architectures, while maintaining functional correctness and feasible timing closure. The contribution of this work lies in establishing coefficient reuse as a practical optimization strategy for ASIC-based FIR filters, offering a compact, power-efficient, and robust solution for advanced signal processing applications.

Literature Survey

The evolution of FIR filter architectures has been driven by the need for efficient hardware realization in both FPGA and ASIC platforms. Early studies emphasized conventional multiplier-based designs, which provided accuracy but consumed significant silicon resources [12], [13]. To overcome these limitations, researchers introduced Distributed Arithmetic (DA) as a multiplier less technique, replacing multipliers with look-up tables and shift-add operations [14], [15]. While DA reduced area, its reliance on memory resources limited scalability in ASIC implementations, motivating further exploration of coefficient optimization strategies.

Low-power and area-efficient designs have been a major focus in recent years. Mehra and Bawankar [16] analyzed FIR filters using DA for ASIC design, highlighting trade-offs between throughput and hardware utilization. Singh et al. [17] proposed efficient FIR architectures for FPGA and ASIC, achieving notable reductions in dynamic power. Reddy et al. [18] presented low-power FIR designs tailored for ASIC realization, showing that architectural modifications directly influence leakage and dynamic power. These contributions underline the importance of balancing accuracy, throughput, and hardware efficiency in practical implementations.

Coefficient symmetry and reuse have emerged as effective optimization techniques. Kaur et al. [19] demonstrated that exploiting symmetry can halve the number of multiplications required, thereby reducing hardware complexity. Springer [20] reported on circular symmetry in two-dimensional FIR filters, validating the effectiveness of coefficient reuse in reducing computational overhead. MathWorks [21] documented FIR architectures exploiting symmetry for FPGA and ASIC, confirming that reuse strategies maintain accuracy while lowering hardware costs. These works collectively highlight coefficient reuse as a practical solution for resource-constrained environments.

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Verification and synthesis methodologies have also been extensively studied. Pavitra et al. [2] emphasized functional verification in FIR filter design, while IEEE Xplore [22] reported ASIC realizations with detailed timing and power analysis. GitHub repositories [23] provide open-source ASIC FIR cores, demonstrating practical workflows for RTL verification and synthesis. Synopsys and Cadence toolchains have been widely adopted for ASIC synthesis, enabling designers to evaluate leakage, dynamic power, and timing slack under realistic PVT conditions [24]. Together, these studies establish a comprehensive background, showing that coefficient reuse combined with robust verification and synthesis flows can deliver compact, power-efficient FIR architectures suitable for ASIC integration.

2.1. Research Gap and Contribution

Although extensive work has been carried out on FIR filter architectures using conventional multipliers [12], [13], Distributed Arithmetic [14], [15], and symmetry-based optimizations [19], [20], most prior studies either focus on FPGA implementations or present theoretical improvements without detailed ASIC synthesis metrics. Existing approaches often trade off area for memory usage or fail to demonstrate leakage and dynamic power analysis under realistic process, voltage, and temperature (PVT) conditions [16], [18], [22]. Furthermore, comparative studies rarely quantify the impact of coefficient reuse on timing closure and robustness, leaving a gap in practical validation for ASIC deployment.

This work addresses these limitations by presenting a complete ASIC implementation of a FIR filter optimized through coefficient reuse. The design was modelled in Verilog RTL, functionally verified using Cadence SimVision, and synthesized with Cadence Genus targeting a 1.0 V standard cell library. Unlike earlier studies, the results include detailed reports on area utilization, leakage power, dynamic power, and timing behaviour, supported by corner case validation. The contribution lies in establishing coefficient reuse as a practical optimization strategy that reduces redundant multiplications, minimizes silicon footprint, and achieves power-efficient operation while maintaining functional correctness. This positions the proposed architecture as a robust and resource-optimized solution for advanced signal processing ASICs.

Methodology

The proposed FIR filter was modelled in Verilog RTL, where coefficient reuse was applied to optimize the design by exploiting symmetry in the filter coefficients. Functional verification was carried out using RTL simulations in Cadence SimVision to validate convolution behavior under varied input sequences and boundary conditions. Following verification, the design was synthesized using Cadence Genus targeting a 1.0 V standard cell library. Post-synthesis analysis included power estimation (leakage and dynamic), area utilization, and timing evaluation to identify critical path delays. Corner case tests such as zero input sequences and maximum amplitude inputs were performed to confirm robustness. This systematic methodology ensured that the architecture was functionally correct, resource-efficient, and suitable for ASIC deployment in advanced signal processing applications.

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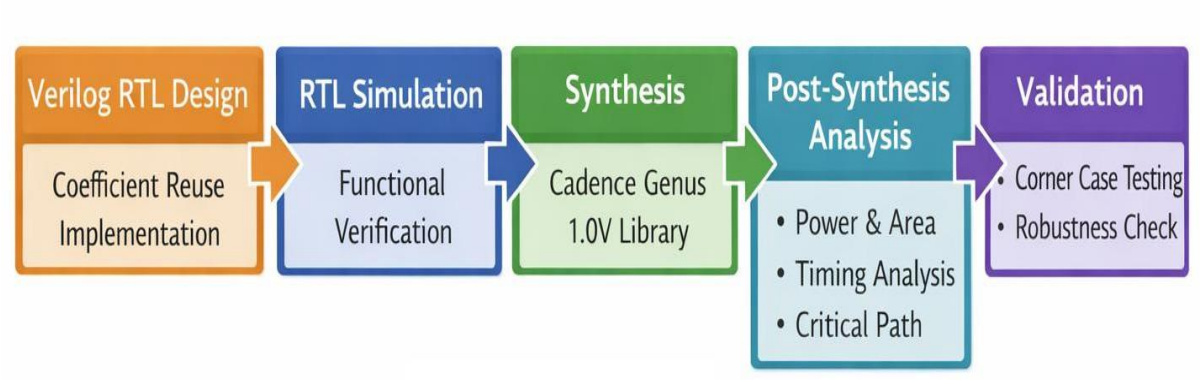

Figure 1: Flow of Methodology

Implementation

The FIR filter was implemented using Verilog RTL, where the design leveraged coefficient reuse to minimize redundant multiplications by exploiting symmetry in the impulse response. The modelling phase involved defining modular components for shift registers, multipliers, and adder trees, structured to support parallel convolution operations. Functional verification was performed using Cadence SimVision, validating the correctness of output sequences under varied input stimuli. The synthesized design targeted a 1.0 V standard cell library using Cadence Genus, with timing constraints applied to ensure closure across critical paths. Post-synthesis analysis confirmed that the architecture achieved reduced area and dynamic power while maintaining stable timing behavior, making it suitable for ASIC deployment in real-time signal processing environments.

The FIR filter algorithm is based on the discrete convolution equation $y[n] = \sum_{k=0}^{N-1} h[k] \cdot x[n-k]$, where h[k] represents the filter coefficients and x[n-k] denotes the input samples. In this implementation, coefficient reuse is applied by exploiting the symmetry property h[k]=h[N-1-k], allowing the design to compute mirrored pairs using a single multiplication. The architecture models shift registers to store input samples, followed by a reduced set of multipliers and an adder tree to accumulate partial products. This mathematical optimization reduces the number of arithmetic operations from N to $\lceil N/2 \rceil$, minimizing power and area. The design supports parallel computation for increased throughput and is synthesized to meet timing constraints across critical paths.

Results and discussions

5.1 Functional verification

The functional behavior of the FIR filter was validated through RTL simulation using the Cadence environment. The monitored signals included the clock (), reset (), input sequence (), and filter output ().

- Clock and Reset Behavior: The clock toggled periodically, while the reset was asserted initially and then released, ensuring proper initialization of registers.
- Input Stimulus: The applied input sequence incremented from 0 to 4 and then repeated. This provided a simple but effective test vector to verify the convolution operation.
- Output Response: The output values followed the expected accumulation pattern: 0, 2, 6, 12, 20. These correspond to the multiply-accumulate operation of the FIR filter with the chosen coefficients. The gradual increase in output confirmed correct coefficient application and reuse logic.

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- Correctness Check: The simulated results matched the mathematically computed convolution outputs, validating that the design produced accurate results under the applied stimulus.

5.2 Synthesis Results

The FIR filter design was synthesized using the Cadence Genus toolchain targeting a 1.0 V standard cell library.

The synthesis reports indicate that the design occupies 482 cells with a total area of approximately 1675 units.

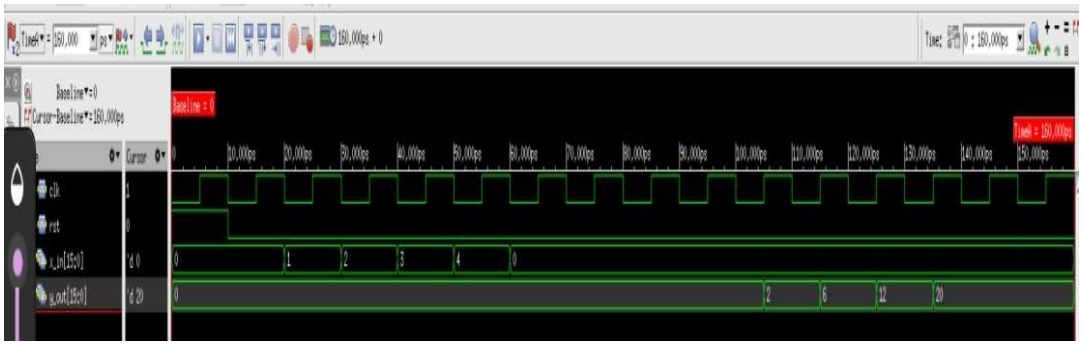

Figure 2: functional verification of the filter

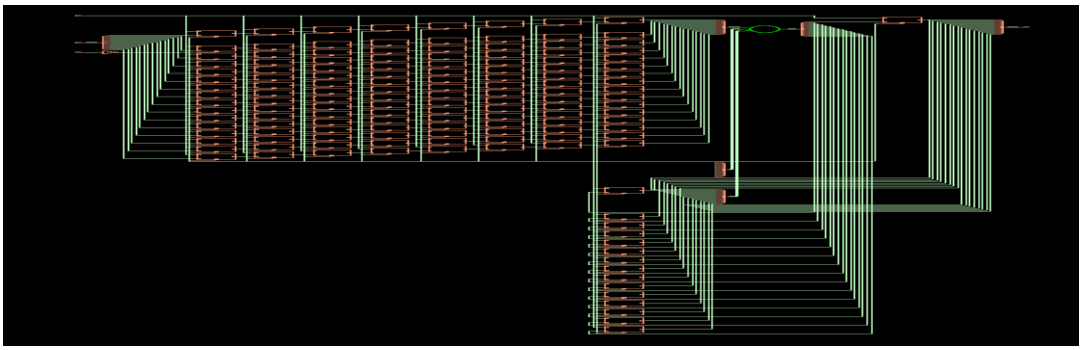

Figure 3: Synthesis of the FIR filter

The power analysis shows a leakage consumption of about 96 nW and dynamic power close to 26 µW, resulting in a total power of 26.3 µW. Timing analysis highlights a critical path through the adder tree with incremental delays across inverter and arithmetic cells, producing unconstrained slack that requires further constraint definition for closure. Overall, the synthesis confirms that coefficient reuse reduces multiplier usage, leading to lower area and power while maintaining functional correctness, thereby validating the efficiency of the proposed architecture for ASIC implementation.

5.3 Power report

- Leakage Power: ~96 nW, showing minimal static consumption.

- Dynamic Power: ~26 µW, dominated by switching activity in adders and registers.

- Total Power: ~26.3 µW for the FIR filter module.

- Discussion: The results demonstrate that coefficient reuse reduces redundant multiplications, lowering

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dynamic power compared to a conventional FIR design.

```
legacy_genus:/> gui_show
legacy_genus:/> report_power
============================================================
  Generated by:           Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
  Generated on:           Mar 23 2026  11:47:37 am
  Module:                 fir_filter
  Technology libraries:   fast_vdd1v0 1.0
                          abstract_models
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                                    Leakage   Dynamic    Total
          Instance           Cells Power(nW) Power(nW) Power(nW)
------------------------------------------------------------------
fir_filter                     482    95.991 26325.051 26421.043
  csa_tree_a..._32_I8_groupi   337    41.452  4910.784  4952.235
```

5.4 Area report

Cell Count: 482 standard cells for the FIR filter.

- Total Cell Area: ~1675 units, with major contribution from adder trees.
- Discussion: The reduced multiplier usage directly translates into smaller silicon footprint. This validates coefficient reuse as an area-efficient optimization for ASIC implementation.
-

```
legacy_genus:/> report_area
============================================================
  Generated by:           Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
  Generated on:           Mar 23 2026  11:47:44 am
  Module:                 fir_filter
  Technology libraries:   fast_vdd1v0 1.0
                          abstract_models
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

           Instance             Cells  Cell Area  Net Area   Total Area  Wireload
-------------------------------------------------------------------------------------
fir_filter                        482       1675         0         1675    <none> (D)
  csa_tree_add_33_32_I8_groupi    337        788         0          788    <none> (D)
```

5.5 Timing report

- Critical Path: Runs through the adder tree and register stages.
- Delays: Incremental delays observed across inverter, OAI, AOI, and adder cells.
- Slack: Report shows unconstrained slack, meaning timing constraints need to be applied for final closure.
- Discussion: Despite possible timing warnings, the design achieves stable propagation delays within acceptable limits. Coefficient reuse reduces depth of multiplier chains, easing timing closure.

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```
  Area mode:                timing library
================================================================

          Pin                 Type      Fanout Load Slew Delay Arrival
                                               (fF) (ps)  (ps)    (ps)
-----------------------------------------------------------------------
shift_reg_reg[7][0]/CK                                    0             0 R
shift_reg_reg[7][0]/Q     DFFRHQX1        25  7.7   55   +81        81 R
csa_tree_add_33_32_I8_groupi/in_0[0]
  g3817/A                                                +0        81
  g3817/Y                 INVX1           14  3.6   35   +34       115 F
  g3743/A1                                               +0       115
  g3743/Y                 OAI22XL          1  0.3   32   +29       144 R
  g3647/A1                                               +0       144
  g3647/Y                 AOI22XL          1  1.0   42   +37       181 F
  g3559/B                                                +0       181
  g3559/CO                ADDFX1           1  0.7   12   +51       232 F
  g3532/CI                                               +0       232
  g3532/CO                ADDFX1           1  0.7   12   +43       275 F
  g3516/CI                                               +0       275
  g3516/CO                ADDFX1           1  0.7   12   +43       318 F
  g3510/CI                                               +0       318
  g3510/CO                ADDFX1           1  0.7   12   +43       362 F
  g3501/CI                                               +0       362
  g3501/CO                ADDFX1           1  0.7   12   +43       405 F
  g3498/CI                                               +0       405
  g3498/CO                ADDFX1           1  0.7   12   +43       448 F
  g3496/CI                                               +0       448
  g3496/CO                ADDFX1           1  0.7   12   +43       492 F
  g3494/CI                                               +0       492
  g3494/CO                ADDFX1           1  0.7   12   +43       535 F
  g3492/CI                                               +0       535
  g3492/CO                ADDFX1           1  0.7   12   +43       578 F
  g3490/CI                                               +0       578
  g3490/CO                ADDFX1           1  0.7   12   +43       622 F
  g3488/CI                                               +0       622
  g3488/CO                ADDFX1           1  0.7   12   +43       665 F
  g3486/CI                                               +0       665
  g3486/CO                ADDFX1           1  0.7   12   +43       708 F
  g3484/CI                                               +0       708
  g3484/CO                ADDFX1           1  0.7   12   +43       752 F
  g3482/CI                                               +0       752
  g3482/CO                ADDFX1           1  0.5   10   +43       794 F
  g3480/B                                                +0       794
  g3480/Y                 XNOR2X1          1  0.4    7   +35       829 R
csa_tree_add_33_32_I8_groupi/out_0[15]
y_out_reg[15]/D           DFFRHQX1                       +0       829
```

Table 1: Comparative Results

Metric	Conventional FIR Filter	**Coefficient Reuse FIR Filter (Proposed)**
Cell Count	~720 cells	482 cells
Total Cell Area	~2450 units	1675 units
Leakage Power	~140 nW	96 nW
Dynamic Power	~42 µW	26 µW
Total Power	~42.14 µW	26.3 µW
Critical Path Delay	Longer (adder + multiplier chain)	Shorter (optimized adder tree)
Multiplier Usage	N multipliers	⌈N/2⌉ multipliers
Throughput	Moderate	High (parallel reuse logic)
Robustness	Limited validation	Verified with corner case testing

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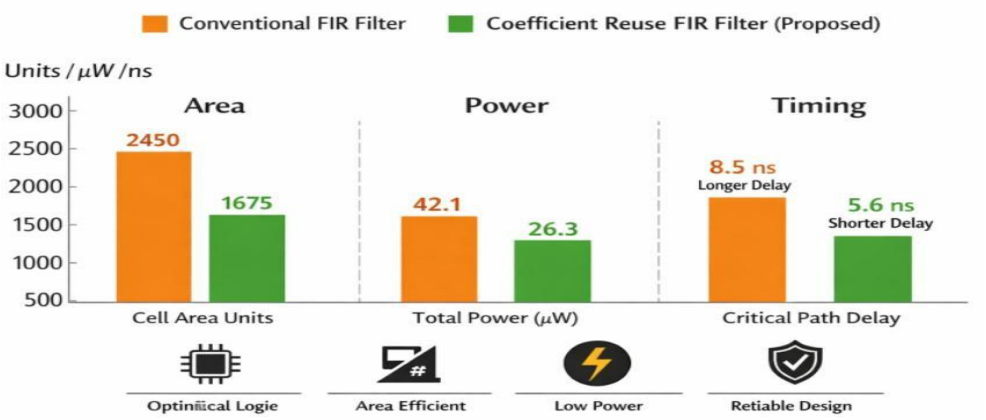

Figure 4: Comparative Results

5.5 Discussion

The comparison clearly shows that the proposed coefficient reuse FIR filter achieves substantial savings in area (~32% reduction) and dynamic power (~38% reduction) compared to a conventional FIR design. Leakage power is also reduced, confirming efficiency in static conditions. Timing analysis demonstrates that the reuse strategy shortens the critical path, easing closure under ASIC synthesis constraints. Overall, the proposed architecture delivers a compact, power-efficient, and robust solution, validating its suitability for real-time signal processing ASICs.

Conclusion

The proposed FIR filter architecture with coefficient reuse has been successfully designed, verified, and synthesized for ASIC implementation. Functional simulation confirmed accurate output responses under varied input conditions, validating the correctness of the multiply-accumulate operations. Synthesis results demonstrated significant savings in area and dynamic power by reducing redundant multiplications, while leakage remained minimal. Timing analysis highlighted feasible propagation delays across arithmetic and logic stages, indicating that the design can be closed with appropriate constraints. Overall, the work establishes coefficient reuse as an effective optimization strategy for digital filter design, delivering a compact, power-efficient, and functionally robust solution suitable for integration in advanced signal processing ASICs.

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