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Research Article

Hardware Implementation of Single-Phase 9-Level Hybrid H-Bridge Multilevel Inverter with Reduced Components

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ABSTRACT

To overcome the disadvantages of conventional Multilevel Inverters (MLI) like requirement of more number of components which will further increase the complexity to generate gate pulses and hence the overall cost, a hybrid topology has been suggested in this paper. Compared to the conventional multilevel inverter, the number of dc voltage sources, switches, installation area, and converter cost is significantly reduced as the number of voltage steps increases. This paper includes the design and simulation of the hybrid converter with different types of PWM techniques. This hybrid converter is a combination of T-Type single phase inverter and H-Bridge module with sub switches. In this hybrid topology, Switching functions are improved in easy way. High quality output voltage wave is obtained in simulation results. It reduces dv/dt stresses experienced by switches and also output voltage harmonic component are low.

Keywords: Hybrid H-Bridge Multilevel Inverter (Hybrid HBMLI), Multilevel Inverter (MLI), Pulse Width Modulation (PWM), Harmonics, Total Harmonic Distortion (THD)

1. INTRODUCTION

In recent years, the use of multilevel inverters increases significantly in different utilities like Renewable Energy conversion system, UPFC, Electrical Vehicles, Motor drives, Distributed Generation, Active Filtering and many other. As compared to two-level inverter, multilevel inverters have lesser Total Harmonic Distortion, Electromagnetic Interference effect, voltage stress across the switch, and higher power rating. A substantial research on topological development of multilevel inverters has been reported in modern days. The objectives of topological improvement are to reduce the number of switching devices and isolated DC power supplies with same number of output voltage levels as compare to conventional MLI topologies [1].

H-bridge Conventional inverters were used in many industrial applications because of their simple switch configuration and easy controlling for many years. But, harmonic components are much more and in some applications their use is not satisfactory [2,3]. Because of the low quality of waveforms of voltage and currents, classic H-bridge inverter has not found huge applications. On the other hand, high switching frequency of PWM inverters and low efficiency results due to their dv/dt stress. Due to these various problems, the conventional H-bridge square wave Inverter and Pulse Width Modulated inverters have been substituted by new multilevel inverters [2-10].

The term multilevel starts from the 3-level inverter. By increasing the number of levels in the inverter, the output voltages have staircase waveforms with numbers of steps generated, harmonic distortion reduces. Although, complexity increases with a high number of levels and issue of voltage imbalance introduces. An effective multilevel inverter should be design in such a way of reducing THD in the output [2].

In modern years, many 1-phase and 3-phase multilevel inverters have been designed and various multilevel switching methods have been investigated. With this point of view, Industrial applications use multi-level inverter

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techniques to decrease the voltage stress developed on power devices and to produce output voltages of good quality. The multi-level inverters improve the ac power quality by performing the power conversion in small voltage steps resulting in lower harmonics content. The lower harmonic content of this output voltage waveform is greatly reduced compared to two-level output voltage waveform [3-17]. Because of its interdisciplinary nature, Power Electronics combines semiconductor devices, digital systems, control theory and power systems. This fact implies that any innovation in one of these fields affects Power electronics and opens new research opportunities.

2. MULTILEVEL INVERTER

The need of multilevel inverter arises due to some well-known disadvantages of conventional Two-level inverters. The advantages of multilevel inverter and basic concept of multilevel inverter is also discussed over here. Classification of multilevel inverters and control techniques are also shown.

Need of Multilevel Inverter

- The output voltage of two-level inverter contains more harmonics.
- PWM-VSIs operating at high switching frequencies are rarely preferred for high power applications due to considerable switching losses.
- PWM-VSIs generate Electromagnetic Interference (EMI).
- As the two-level inverters have to switch between the two extreme levels of the dc-link voltages, they are subjected to High dv/dt.
- The task of reducing harmonic content in the output voltage is addressed by the multilevel inverters.
- Multilevel inverters are realized from a number of smaller discrete voltage sources, and they generate the output voltage waveforms with more steps of smaller magnitudes approaching sine wave.

Advantages of Multilevel Inverters [11]

- They are suitable for high-voltage and high-current applications.
- They have reduced Total Harmonic Distortion (THD) in voltage with increased number of voltage levels.
- They can be operated with the lower switching frequency and hence the switching losses are reduced.
- They have higher efficiency.
- Power Factor is close to unity for MLIs used as rectifier.
- No Electromagnetic Interference (EMI) problem exists.
- It is possible to use power semiconductor devices of lower voltage ratings to realize high voltage levels at inverter output.

Classification of Multilevel Inverter

The classification of multilevel inverters based on number of dc sources used is given the Fig. 1. [10]

Multilevel Inverter Modulation Techniques

The output voltage obtained in the multilevel inverter depends on the control technique used. Different modulation methods are used to control the output voltage of the multilevel inverter [4]. The modulation methods for multilevel inverter based on switching frequency are classified as shown in Fig. 2.

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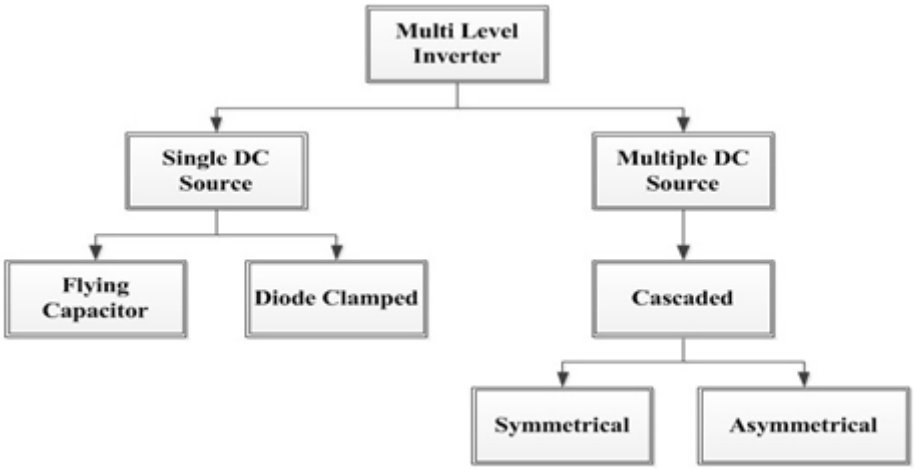

Fig. 1. Classification of Multilevel Inverter

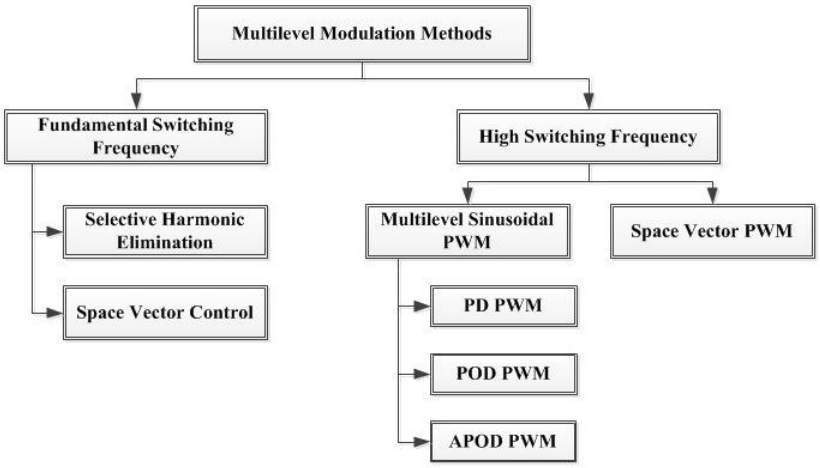

Fig. 2. Multilevel Inverter Modulation Techniques

Features of Multilevel Inverter

- The output voltage and power increase with number of levels.
- Increasing output voltage and power does not require any increase in rating of individual device.
- The harmonic content decreases as the number of levels increases and filtering requirements decreases.
- With additional voltage levels, the voltage waveform has more free-switching angles, which can be preselected for harmonic elimination.
- In the absence of any PWM techniques, the switching losses can be avoided.

Problems with Conventional Multilevel Inverter

The problems with conventional multilevel inverters can be summarized as follows.

- Conventional topologies of Multilevel Inverters use more number of power switches. Its output voltage waveform may contain more harmonics.
- It has been seen that, with increase in number of output levels, the numbers of clamping diodes in Diode Clamped inverter and the storing capacitors in Flying-Capacitors inverter increases.

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- The inverter control can be very complicated in Flying-Capacitors inverter.
- Cascaded inverter needs separate dc sources for real power conversion

3. HYBRID MULTILEVEL INVERTER

To overcome the problems with conventional multilevel inverters, one hybrid topology of multilevel inverter is discussed here. Objectives of Hybrid H-Bridge Multilevel Inverter (Hybrid HBMLI) are given as follows.

Objectives of Hybrid HBMLI

- To have high quality output voltage with less THD.
- It must contain less number of power semiconductor switches and other components.
- It should have quite simple principle of operation.
- It should have implementable switching strategy.
- It should have low dv/dt stress on power semiconductor devices

Topology of Hybrid HBMLI

The topology of Hybrid Cascaded H-Bridge Multilevel Inverter containing two dc sources, two capacitors and seven switches is shown in Fig. 3. As the magnitude of both the sources is equal the topology is considered as Symmetrical Hybrid Cascaded H-Bridge Multilevel Inverter.

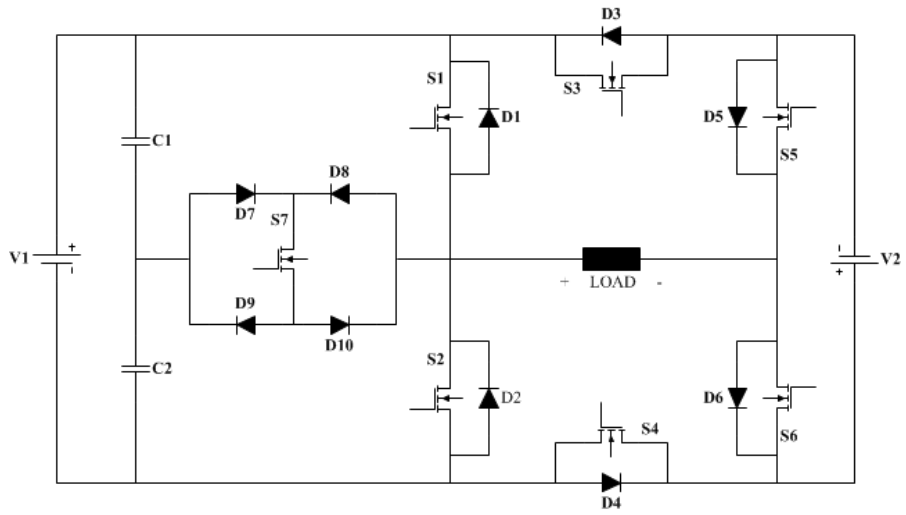

Fig. 3.Symmetrical Hybrid H-Bridge Multilevel Inverter

Components Requirement Analysis

The requirement of components for Hybrid HBMLI is analyzed as follows.

Let, m = Number of levels in output,

Consider m = 9

Let, s = Total number of power switches required, It can be calculated by

$s = (m + 19) \div 4$

Putting m = 9, we get

$s = (9 + 19) \div 4 = 28 \div 4 = 7$

Hence, total number of power switches required, ***s = 7***.

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Let, d = Total number of diodes required, It can be calculated by

$d = m + 1$

Putting m = 9, we get, d = 10

Hence, total number of diodes required, ***d = 10***.

Let, c = Total number of dc link capacitors required, It can be calculated by

$c = (m - 1) \div 4$

Putting m = 9, we get, c = 2

Hence, Total number of capacitors required, ***c = 2***.

Comparison of Components Requirement per Leg of MLI

From the analysis of requirement of components for Hybrid HBMLI, it is now become possible to compare it with the requirement of components for conventional MLI. Comparison of number of components required for conventional multilevel converters and Hybrid HBMLI for 9-level is given in the TABLE I.

TABLE I : Comparison of Components Requirement per leg of 9-level MLI

Component	Type of Converter (MLI)			
	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Hybrid H-Bridge
Main Switching Devices	16	16	16	7
Main Diodes	16	16	16	10
Clamping Diodes	56	0	0	0
DC bus Capacitors	8	8	0	2
Balancing Capacitors	0	28	0	0
Isolated DC Sources	1	1	4	2
TOTAL	97	69	36	21

Working Principle

The working principle of Hybrid HBMLI can be explained simply with the help of the switching table. If the switch is in state "1" then it is considered that switch is conducting. Similarly if the switch is in state "0" then it is considered that switch is not conducting. The TABLE II shows the switch states according to which the desired output voltage waveform is generated.

TABLE II : Switching Table

Mode	Output Voltage V_o Volts	Switch State						
		S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	0 V	0	0	1	0	0	0	0

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		0	0	0	1	0	0	0
1	+24 V	0	0	0	1	0	0	1
2	+48 V	0	0	0	1	1	0	0
3	+72V	0	0	0	1	1	0	1
4	+96 V	1	0	0	1	1	0	0
5	-24 V	0	0	1	0	0	0	1
6	-48 V	0	0	1	0	0	1	0
7	-72 V	0	0	1	0	0	1	1
8	-96V	0	1	1	0	0	1	0

4. SIMULATION RESULTS

Sine-wave of fundamental frequency (50Hz) is compared with level shifted triangular carrier waves of 1 kHz frequency. The comparator output is further processed to generate the required gate pulses. The gate pulses are then applied to the respective switches of the power circuit. Simulation results for resistive load are shown in Fig. 4 to Fig. 7 for modulation index Ma = 1.05625. The output waveform is optimized and has THD of 9.51% which is very less than that of conventional MLIs. Fig. 4 shows the comparison of multiple carrier waves with the fundamental sine wave, Fig. 5 shows the applied gate pulses to the power semiconductor switches of MLI, Fig. 6 shows the output voltage and current waveforms of the MLI for resistive load of 10 Ω, Fig. 7 shows the FFT analysis of output voltage waveform. The FFT analysis for output current waveform is same as the output voltage waveform due to resistive load.

Simulation Results with POD PWM for Resistive Load (M_a= 1.05625)

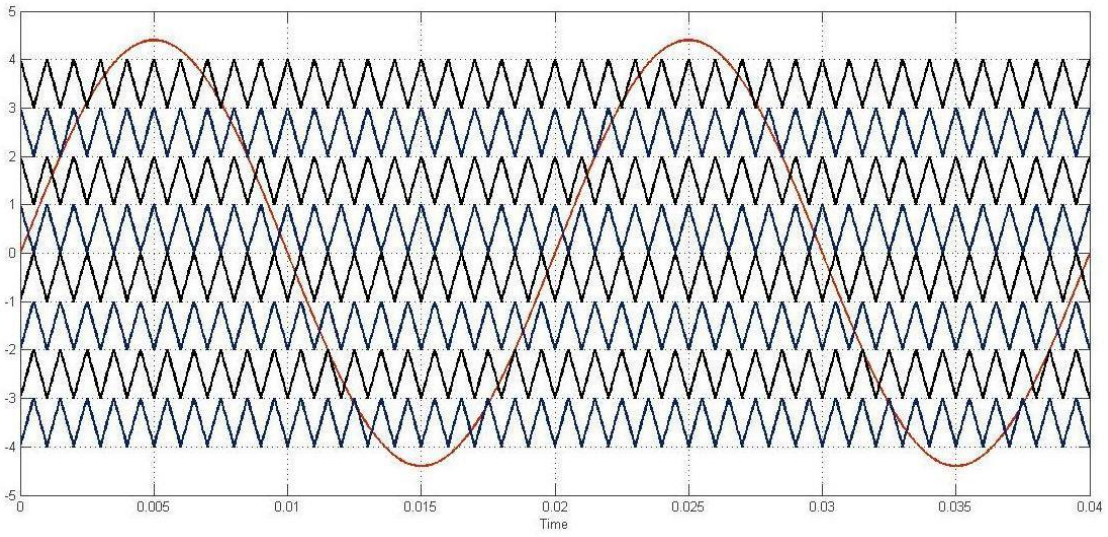

Fig. 4. Comparison of Multiple Carrier Waves with Sine Wave

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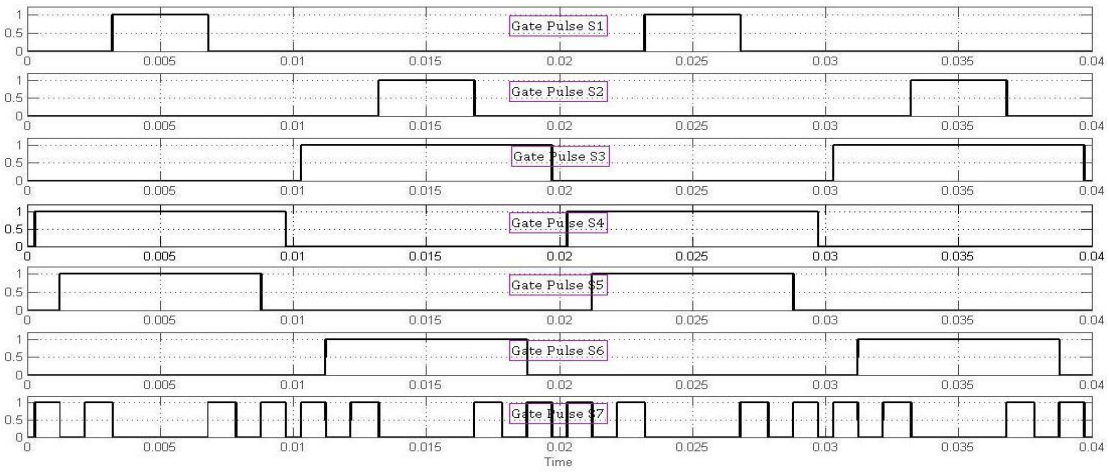

Fig. 5. Gate Pulses

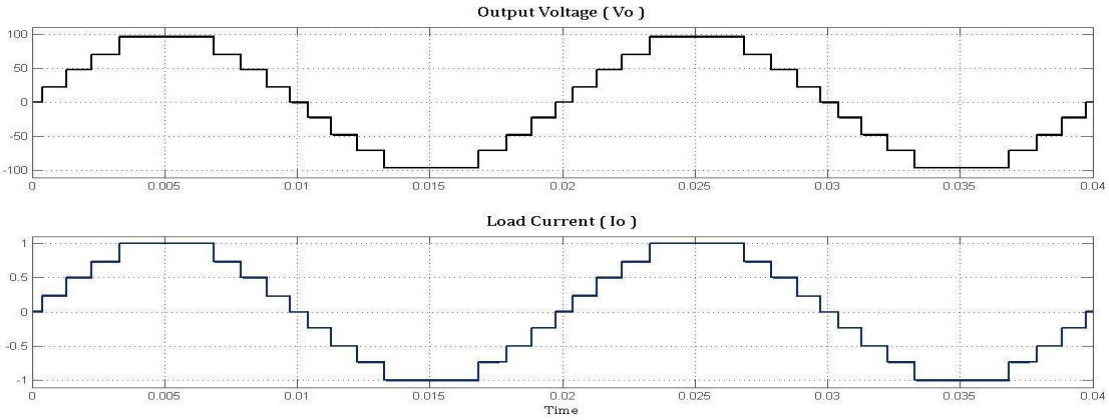

Fig. 6. Output Voltage and Current Waveforms for Resistive Load

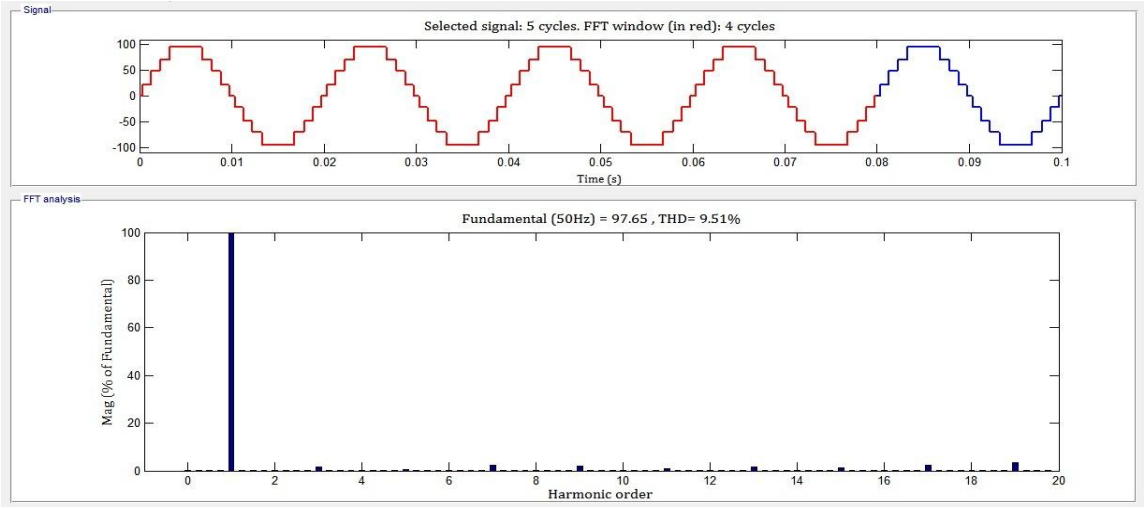

Fig. 7. FFT analysis of voltage waveform

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Comparison of THD for Different PWM Techniques

After applying various pulse width modulation techniques for Hybrid HBMLI with different modulation index the readings of THD were noted down and it is given in TABLE III. It shows the POD PWM method is giving 11.03% THD with Modulation Index of 1 and hence best suited for the Hybrid HBMLI.

TABLE III : Comparison of THD for Different PWM Techniques

Modulation Index	Total Harmonic Distortion (THD) %				
	APOD	POD (Initial zero coincide)	PD	VAPOD	POD
0.8	16.52	15.66	16.89	16.81	18.06
0.9	17.18	18.25	16.95	17.85	15.79
1.0	14.96	17.18	14.67	18.07	11.63
1.1	11.84	12.31	11.75	17.93	11.03
1.2	12.77	11.53	12.93	18.18	14.15

5. HARDWARE SET-UP RESULTS

The experimental set-up for the testing of Hybrid HBMLI is shown in the Fig. 8.

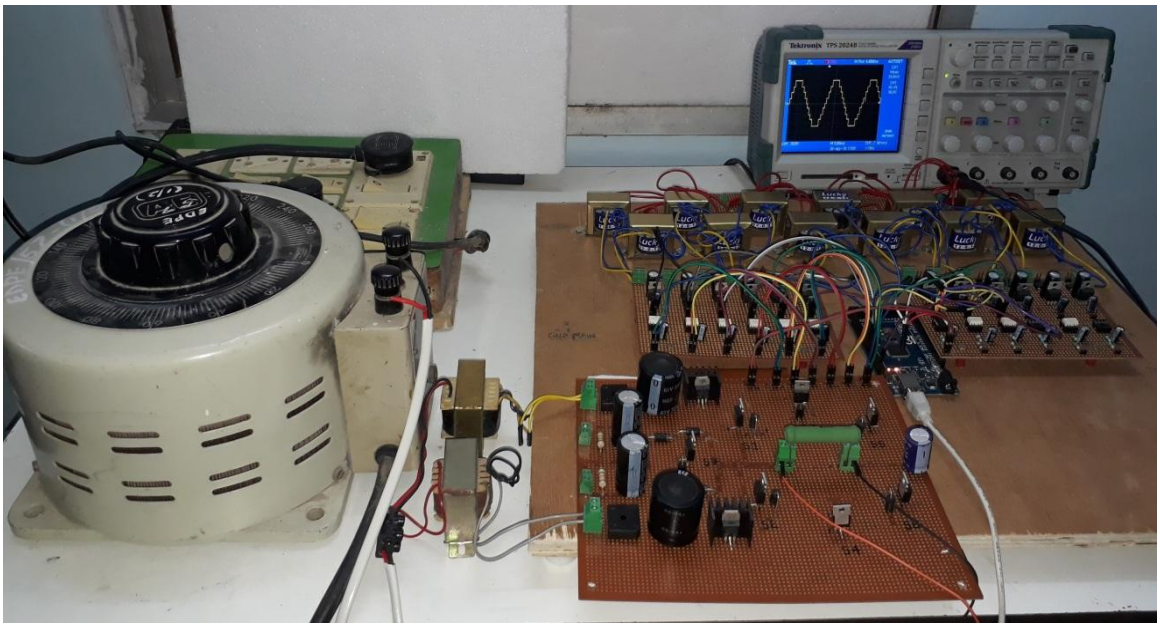

Fig. 8. Experimental Set-up for Testing of Hybrid HBMLI

Hardware Test Results

The results obtained for gate pulses at d SPACE ADC output port are measured with DSO and are shown in the Fig. 9.

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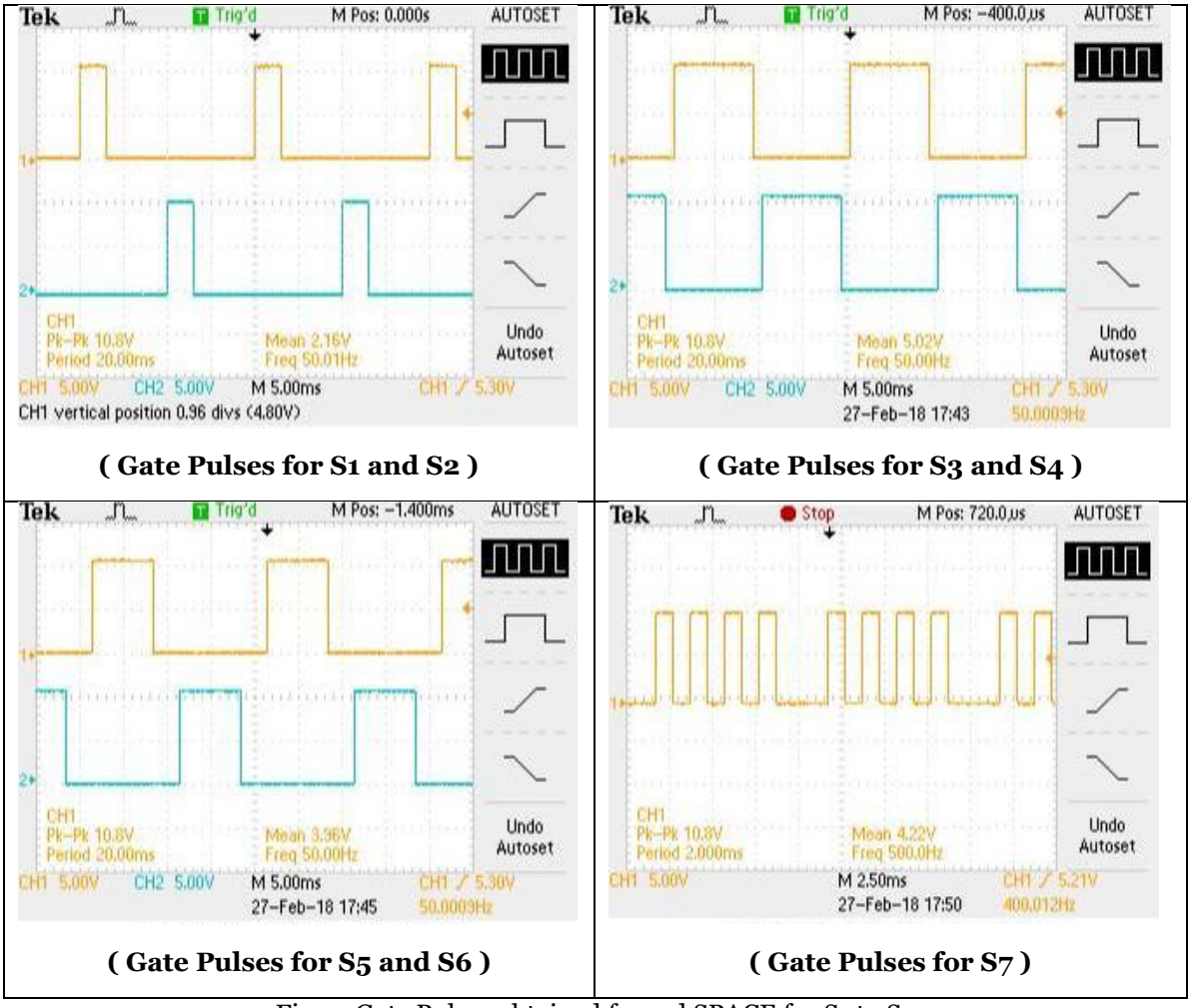

Fig. 9. Gate Pulses obtained from d SPACE for S1 to S7

The output voltage across the load resistor of 1 KΩ is measured using DSO andis shown in Fig. 10.

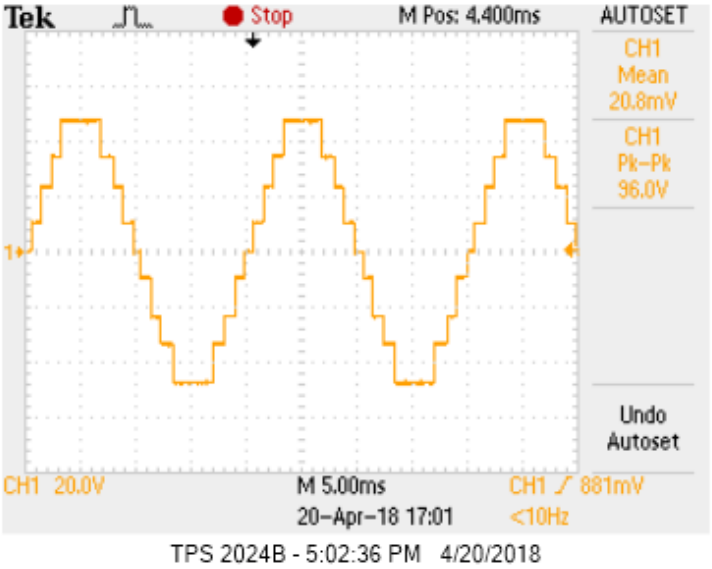

Fig. 10. Output Voltage Waveform (Time Base = 5 ms)

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The FFT analysis of the hardware output voltage waveform is shown in the Fig. 11.FFT analysis shows that the output voltage has the THD of 10.53%.

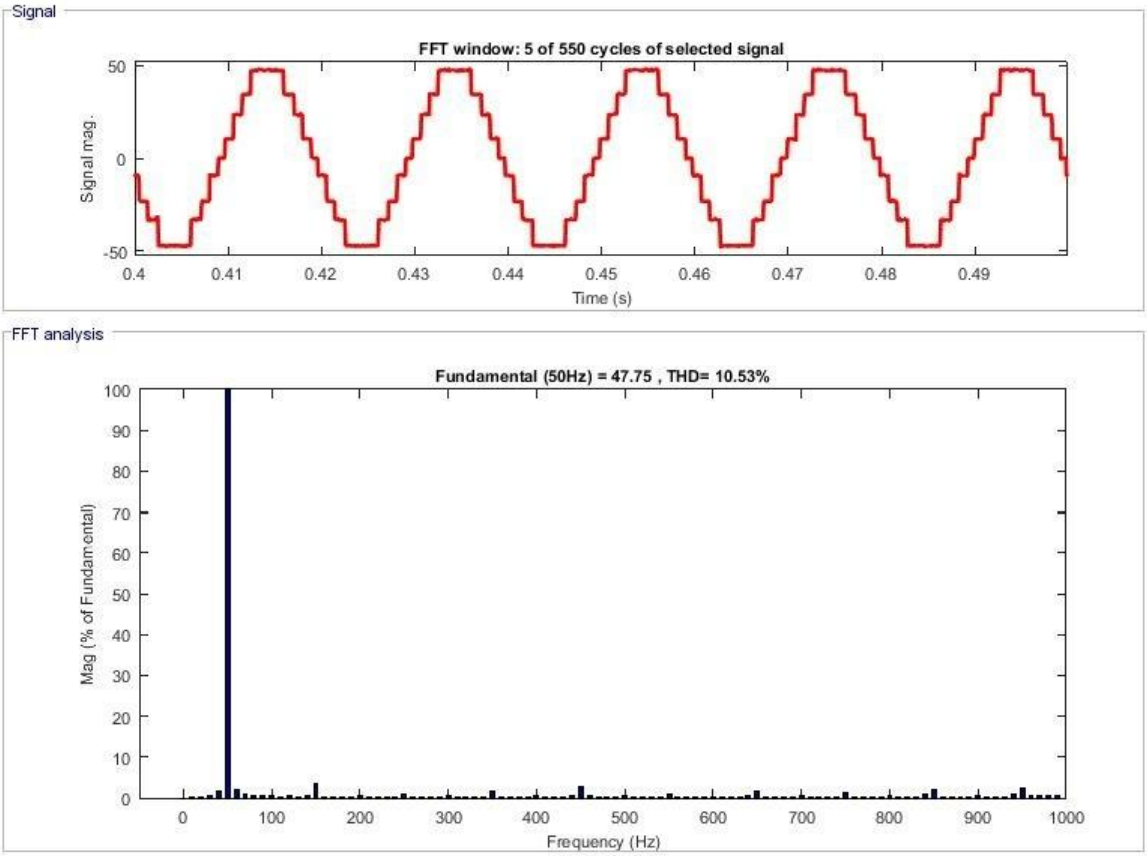

Fig.11. FFT Analysis of Output Voltage

Comparison of Hardware results with Simulation results.

The result obtained with hardware and simulation for Hybrid HBMLI using POD PWM control method is compared. The comparison is shown in the Table IV.

Table IV :Comparison of Hardware results with Simulation results

Modulation Index	Simulation results			Hardware results		
	Peak-to-Peak Voltage	RMS Voltage	THD %	Peak-to-Peak Voltage	RMS Voltage	THD %
1.05625	96 V	48.67	9.94	96 V	47.75	10.53

6. CONCLUSION

From the work done so far it can be concluded that, the proposed 9-level Hybrid HBMLI requires a total of 21 components which is quite less than that of conventional MLIs. The harmonic content in the output of 9-level Hybrid HBMLI is 9.51% which is almost 2% less than that of 9-level Cascaded H-Bridge MLI. The hardware results are also satisfactory with the THD of 10.53%.

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REFERENCES

[1] Shouvik Mondal, Tapas Roy, Abhijit Dasgupta, and Pradip Kumar Sadhu “Study of a New Single Phase Multilevel Inverter based on Switched Capacitor Units” 1st IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES-2016).

[2] Bhabani Shankar P., Debendra Kumar Dash, Joydeep Mukherjee “Implementation of PWM Based Firing Scheme for Multilevel Inverter Using Microcontroller” National Institute of Technology, Rourkela. 2009.

[3] S.Çamur, B.Arifoglu, E. Kandemir Beser and E.Beser “A Novel Topology for Single-Phase Five level Inverter Compared With H-Bridge Inverter” International Symposium on Power Electronics, Electrical Drives, Automation and Motion SPEEDAM 2006.

[4] Adithya S. N. and Raghu Raman S. “Study of Multilevel Sinusoidal PWM methods for Cascaded H-Bridge Multilevel Inverters” 2014 IEEE 2nd International Conference on Electrical Energy Systems (ICEES).

[5] Charles I. Odeh, Damian B. Nnadi and Emeka S. Obe “Three-phase, Five-level Multi-level Inverter Topology” Electric Power Components and Systems, Taylor & Francis Group, LLC, 40:1522–1532, 2012.

[6] S. K. Rai, Pradyumn Chaturvedi, Shimi S. L. “SHE-PWM Based Multilevel T-Type Inverter Topology for Single-Phase Photovoltaic Applications”. IEEE Transactions, 978-1-4673-8888-7/16@2016.

[7] Gnana Prakash M, Balamurugan M, Umashankar S. “A New Multilevel Inverter with Reduced Number of Switches”. International Journal of Power Electronics and Drive System (IJPEDS) Vol. 5, Special Issue on Electric Power Converter, July 2014.

[8] J. Swetha, S. Zubeda, Ch. D. Lakshmi Priya, and B. M. Reddy “A Three Phase Cascaded H-Bridge Multi Level Inverter fed Induction Motor Drive with Reduced Switches”. SSRG International Journal of Electrical and Electronics Engineering– (ICEEMST’17) - Special Issue- March 2017.

[9] Pratik Udakhe, Dipesh Atkar, Sateesh Chiriki, and V. B. Borghate “Comparison of Different Types of SPWM Techniques for Three Phase Seven Level Cascaded H-Bridge Inverter”. 1st IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES-2016).

[10] Jose Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng “Multilevel Inverters: A Survey of Topologies Controls, and Applications”. IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 4, AUGUST 2002

[11] Muhammad H. Rashid “Power Electronics: Circiuts, Devices and Applications” 3rd Edition, Pearson Education.

[12] Dwivedi, Arpan, and Yogesh Pahariya "Design and analysis of hybrid multilevel inverter for asymmetrical input voltages." Journal of Electrical Engineering & Technology 16.6 (2021): 3025-3036.

[13] Al-Hitmi, Mohammed A., et al. "Symmetric and asymmetric multilevel inverter topologies with reduced device count." IEEE Access 11 (2022): 5231-5245.

[14] Das, Madan Kumar, et al. "Generalized Hybrid Symmetrical and Asymmetrical Multilevel Inverter Topology with Reduced Number of Switches." Sustainable Energy and Technological Advancements: Proceedings of ISSETA 2021. Singapore: Springer Singapore, 2022. 81-94.

[15] Mahato, B., Majumdar, S., Jana, K.C. et al. “A Generalized Series-Connected Multilevel Inverter (MLI) Based on Reduced Power Electronic Devices for Symmetrical/Asymmetrical Sources.” Arab J Sci Eng 48, 5907–5924 (2023). https://doi.org/10.1007/s13369-022-07066-z

[16] V. Kubendran, Y. Mohamed Shuaib, S. Vidyasagar, V. Kalyanasundaram, K. Saravanan, “The development of a generalized multilevel inverter for symmetrical and asymmetrical dc sources with a minimized ONstate switch,” Ain Shams Engineering Journal, Volume 15, Issue 2, 2024, 102358, ISSN 2090-4479, https://doi.org/10.1016/j.asej.2023.102358.

[17] A. P. Patel, V. J. Rupapara and A. R. Gauswami, "Design and Simulation of 9-Level Hybrid Cascaded H-Bridge Multilevel Inverter with Reduced Components," 2018 International Conference on Current Trends towards Converging Technologies (ICCTCT), Coimbatore, India, 2018, pp. 1-7, doi: 10.1109/ICCTCT.2018.8551027.