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Research Article

An Explainable AI-Driven Framework for Functional Verification and Hardware Trojan Detection in Next-Generation System-on-Chip Architectures

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ABSTRACT

The rapid growing complexity of next-generation System-on-Chip (SoC) architectures has sharply increased the problem of functional assurance and hardware security, especially on the detection of stealthy Hardware Trojans (HTs). Conventional methods of verification do not detect triggers of rare events as well, and have no transparency in decision making procedures. To overcome these drawbacks, this paper suggests an original Explainable Artificial Intelligence (XAI)-based framework to support unified functional verification and hardware Trojan detection of the SoC designs. The suggested implementation combines anomaly detection on a case of deep learning and interpretable mechanisms to report sensible information to design suspicious behavior. The framework codes on structural and functional characteristics derived using Register Transfer Level (RTL) and gate-level models, permitting the identification of rogue breaches at an early stage. In addition, the XAI models like feature attribution and attention visualization are introduced to promote the trust, debugability, and efficiency of verifying. The offered framework, in contrast to the traditional black-box AI models, is transparent, as the key elements and signal-tracing directions leading to the activities of Trojan are identified. This paper describes a scalable, technology-neutral architecture that can be incorporated into more current Electronic Design Automation (EDA) processes. The proposed framework will make the gap between AI-based security analysis and verification needs closer, which will create the path to more secure and reliable SoC design approaches.

Keywords: Explainable AI, Hardware Trojans, System-on-Chip (SoC), Functional Verification, XAI, Deep Learning, EDA, Hardware Security.

1. INTRODUCTION

THE swift semiconductor technology has facilitated the incorporation of billions of transistors on a single chip and has produced extremely complicated and heterogeneous System-on-Chip (SoC) frameworks [1], [6]. They have become popular in such high-development settings as autonomous systems, health devices, aerospace systems, and secure communication systems. Although this evolution has brought tremendous changes in the aspect of the computational performance, energy and efficiency of the system, it has equally created a lot of problem in the aspect of the verification of the functionality as well as the security of the hardware.

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The functional verification stage is a critical design phase of SoCs, which takes up to a large part of the total development duration and expense. As the complexity of design rises, it is tricky to make certain that it is correct at all operational scenarios. Traditional verification methods, such as simulation-based testing, formal verification and coverage-based methodologies typically do not scale very well with the size and complexity of current SoCs [3]. Such constraints lead to attainment of incomplete verification coverage and heighten chances of unnoticed design defects.

Simultaneously, hardware security is now a major issue because of the globalization of semiconductor design and the extensive adoption of third party intellectual property (IP) cores [6]. This distributed system of designing and fabrication is vulnerable to malicious changes referred to as Hardware Trojans (HTs) [1]. Hardware Trojans are deliberate malicious modifications in a circuit which may cause soccer disruption, release sensitive data, or weaken system performance [2]. The reason as to why these Trojans are normally programmed to stay dormant under normal operating conditions and only rise when particular and uncommonly occurring circumstances are satisfied is that detection is very difficult.

Historical hardware Trojan detection methods are based on side-channel examination, structural examination, and functional examination [5]. These techniques however have a common setback of low sensitivity of the techniques, high rates of false-positives as well as failure to detect advanced Trojans which are deep-rooted in multi-component designs [4]. In addition, most of these methods are executed in later design flow phases, which decrease their utility and create a higher expense of mitigation.

Over the past several years, the concepts of Artificial Intelligence (AI) and Machine Learning (ML) have been promoted as effective instruments to deal with various issues of complex pattern recognition and anomaly domain [7], [15]. Within the framework of hardware security, AI-based methods have shown potentials of detecting a subtle anomaly in circuit behavior and circuit structure patterns potentially indicating hardware Trojans [7]. Deep neural networks, graph-based learning and data driven classification methods have been studied to improve the accuracy of detection and scalability [9].

In spite of such improvements, one of the major constraints of current AI based solutions is the inability to exploit black-box models. These models are very accurate in prediction but they are not interpretable and engineers find it hard to know the logic behind the decision that the models make [11]. Where this attribute is not crucial, e.g., in safety-critical applications where verification and validation are important, explain ability becomes absent making the model outputs less trustworthy and inhibiting their effective implementation. Verification engineers not only need proper detection mechanisms, but also clear understanding of the reason why a specific component or signal has been detected as suspicious.

Explainable Artificial Intelligence (XAI) has attracted significant interest to deal with this issue, as a way of enhancing both transparency and interpretability in AI systems [12], [13]. XAI works like feature attribution, saliency maps, and attention mechanisms can be used because XAI techniques allow their use to explain model predictions in human-understandable terms. Enabling hardware verification to include XAI allows the gap between automated detection and a human-initiated analysis, facilitating more trust and debuggability and decision-making.

Here the present paper already suggests a new Explainable AI-based system of functional checking and Trojan hardware recognition in the next-generation SoC systems. The suggested framework will be used to consolidate verification and security analysis, where AI models will be used as the core of anomaly detection and, at the same time, trying to explain why they make certain decisions, which can be understood. The framework works at various levels of abstraction, such as Register Transfer Level (RTL) and gate-level description, hence identifying the possible threats in the design phase sooner.

As opposed to the traditional methodologies, the advanced framework focuses on the accuracy of

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detection as well as explain ability. Through the XAI techniques, integrating value-added tools within the framework helps illuminate vital feature, signal connections, and structural elements that lead to suspiciousness. Not only is the detection of hardware Trojan facilitated by this, but effective debugging and root-cause investigation are also supported by it. Moreover, the framework is modeled to be scalable and in equivalence with current Electronic Design Automation (EDA) software, which predetermines its suitability to use it in real design settings.

The most significant contributions of the paper may be highlighted as following:

- A watchdog infrastructure that, to an extent, combines both functional verification and hardware Trojan detection.
- Use of Explainable AI methods to improve ownership and trust in AI-based analysis.
- Supply-Based multi-level analysis approach using RTL and gate-level functionality.
- Technology-agnostic scalable architecture, supported by current EDA processes.
- An organized approach to better verification coverage and prompt threat detection.

The rest of this paper will run in the following format: the II part will be a detailed review of the literature on the related work in hardware Trojan detection and AI-based verification techniques. The III section is the formation of the problem and research obstacles. In Section IV, the offered Explainable AI-driven framework is detailed. The methodology and implementation aspects are discussed in section V. Section VI gives the expected results and possible limitations discussion and Section VII gives the conclusion of the paper with the future research.

2. RELATED WORK

Functional verification and hardware Trojan detection have been a gathering topic of central concern in the last few years in the context of System-on-Chip (SoC) architectures [1], [6]. As integrated circuit designs and supply chains of semiconductor manufacturing became more and more complex and globalized, researchers have presented numerous methods that start with the common methods of traditional verification to advanced techniques based on both Artificial Intelligence (AI) and Artificial Intelligence (AI).

A. Hardware Trojan Detection Techniques

Hardware Trojans (HTs), which are lethal to integrated circuit security and reliability, are a serious issue [1]. Side-channel analysis as a primary approach to early detection techniques was mainly based on power consumption and timing behavior analysis and electromagnetic emissions [2]. These techniques are trying to detect anomalies through the comparison of the properties of a suspected chip with a trusted reference design. Nevertheless, these methods are usually affected by inconsistencies in the process and environmental interference, that may result in faulty identification.

Structural analysis methods have also been extensively studied in which the circuit netlist is subjected to structural analysis to identify suspicious components or untapped logic, which may point to Trojan insertion [3]. Although they offer an enhanced visibility of the design structure, they do not do much in locating the highly stealthy Trojan which is thoroughly integrated into the logic of the normal design.

The functional testing techniques, such as to Automatic Test Pattern Generation (ATPG) can be used to trigger the infrequent Trojan triggering conditions [4]. These methods are effective in some situations, but they do not scale well or have coverage especially in large-scale designs of SoCs. Consequently, the traditional methods can sometimes not offer full protection against advanced hardware Trojans.

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TABLE I: COMPARISON OF EXISTING APPROACHES FOR HARDWARE TROJAN DETECTION AND FUNCTIONAL VERIFICATION

Approach	**Technique Used**	**Detection Capability**	**Scalability**	**Explain ability**	**Limitations**
Side-Channel Analysis [2], [5]	Power, timing, EM analysis	Moderate (detects active Trojans)	Low	No	Sensitive to noise and process variations
Structural Analysis [3]	Netlist inspection, pattern matching	Limited(misses stealthy Trojans)	Moderate	Partial	Ineffective for deeply embedded Trojans
Functional Testing (ATPG) [4]	Test pattern generation	Low to Moderate	Low	No	Poor coverage of rare trigger conditions
Traditional ML Models [7]	SVM, Random Forest, ANN	Moderate	Moderate	No	Requires manual feature engineering
Deep Learning Models [9], [15]	CNN, RNN, DNN	High	High	No	Black-box nature, lack of interpretability
Graph-Based Learning [9]	GNNs for circuit graphs	High	High	Limited	Complex implementation, limited explain ability
ML-based Verification [7]	Coverage prediction, bug detection	Moderate	High	No	Focuses on Performance not security
Explainable AI (XAI) Approaches [12], [13]	SHAP, LIME, Attention	High (with insights)	Moderate	Yes	Still emerging, lacks unified frameworks
Proposed Framework	**AI + XAI Integra-tion**	**High**	**High**	**Yes**	**Conceptual (no implementation yet)**

B. *AI-Based Approaches for Hardware Security*

In order to address the shortcomings of conventional tooling, scholars have been progressively embracing the Artificial Intelligence (AI) and Machine Learning (ML) mechanisms to hardware security [7]. Circuit classifications have been done using supervised learning model, like Support Vector Machines (SVMs), Random Forests, and Artificial Neural Networks (ANNs).

In recent days, deep learning methods have become more popular because they are capable of automatically learning complicated patterns with large data sets [9]. Circuit layout spatial features have been analyzed with Convolutional Neural Networks (CNNs) and temporal circuits analyzed with Recurrent Neural Networks (RNNs). Graph Neural Networks (GNNs) become a strong resource of modelling circuit netlists and gain a deeper insight into the relational structure of components [9]. Although they are more accurate, most AI-based techniques are black-box models and give no or

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minimal understanding of the rationale that caused the prediction [11]. This interpretability restricts their use in real workflows of verification, where as much as it is important to identify anomalies, it is also important to understand the cause of the anomaly.

C. Explainable AI in Hardware Security

Explainable Artificial intelligence (XAI) has become a response to these interpretability issues that characterized models of black-box AI [12], [13]. Methods or tools like Local Interpretable Model-agnostic Explanations (LIME), Shapley Additive explanations (SHAP), and attention gain an understanding of the importance of features and how the decision-making is done. XAI has been used to determine critical features and areas in a circuit which can lead to anomalous behavior in the context of hardware security [11]. The explanations will help the verification engineers to know possible vulnerabilities as well as to trace the root cause of anomalies reported. Even though it is a young discipline, XAI has demonstrated high potential in enhancing trust and usability of AI-powered security models.

RESEARCH GAP

Even though the software part of hardware Trojan's detection and AI-Based verification advances, there are still multiple issues. The current solutions are not fragmented because most of the solutions address functional verification and hardware security as independent issues. Also, AI models cannot be explained and this fact undermines their use in safety-critical design procedures.

It is apparent that the need is to have an all-in-one framework that unites functional verification and hardware Trojan detection and able to give insightful understanding of the analysis procedure. This loophole drives the proposed Explainable AI-based architecture, which promises to synthesize the accuracy in detection with the transparency and pragmatic usability within the current SoC design processes.

Textual examination of Table I below shows the weaknesses and strength of modern methods of detecting hardware Trojan and functional verification. Conventional methods like side-channel analysis and functional testing are rather inflexible in terms of scalability and are unable to identify stealthy Trojans, especially those which are triggered by exceptional circumstances. The conventional approaches to structural analysis offer medium-level of visibility but cannot reveal long-running difficult to detect malicious code. Machine learning, and deep learning-based systems, on the other hand, have better detection properties and can scale, but are to a large extent black-box models, which are difficult to interpret and impossible to understand. Graph-based learning methods further improve the sensitivity of detection by modeling circuits relationships though it brings extra complexity and still has limited explain ability. Although there is a growing subdiscipline of Explainable AI (XAI) that deals with the interpretability issue of models by offering understanding of decisions made by models, they are isolated and not cohesively integrated into a comprehensive verification system. The proposed framework as presented in the table stands out due to possessing high capability of detection, scalability and explain ability in one framework as illustrated in the table. This combined methodology is a remedy to the major weaknesses of previous research because it allows both reliable identification and resultant insight, which is more applicable in practical implementation of the approach in current SoC verification and security processes.

3. METHODOLOGY

This section presents the proposed semi-practical methodology for an Explainable AI-driven framework aimed at functional verification and hardware Trojan detection in next-generation System-on-Chip (SoC) architectures. Unlike purely theoretical approaches, the proposed methodology assumes a realistic verification environment where design data, simulation traces, and benchmark datasets (e.g., Trust-Hub benchmarks) are available for training and evaluation.

The framework integrates data preprocessing, feature engineering, AI-based anomaly detection, and

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explainable AI (XAI) into a unified verification pipeline. The goal is not only to detect hardware Trojans but also to provide interpretable insights that assist verification engineers in identifying the root cause of anomalies.

A. ***System Overview and Problem Formulation***

The detection of hardware Trojans in SoC designs can be formulated as a supervised or semi-supervised learning problem. Given a set of circuit designs, the objective is to classify each design (or its components) as either *benign* or *Trojan-infected*, while also providing an explanation of the decision.

Let the dataset be defined as:

$$D = \{(x_i, y_i)\}_{i=1}^{N} \quad \text{1....}$$

Where,

- $x_i \in R^d$ represents the feature vector extracted from the i^{th} circuit
- $y_i \in \{0, 1\}$ represents the class label (0 = normal, 1 = Trojan)
- N is the number of samples

The goal of the model is to learn a mapping function:

$$f(x_i; \vartheta) = \hat{y}_i \quad \text{2...}$$

where θ represents model parameters and $\hat{y}_i$ is the predicted probability of Trojan presence. To optimize the model, binary cross-entropy loss is used:

$$L = -\frac{1}{N}\sum_{i=1}^{N}[y_i \log(\hat{y}_i) + (1 - y_i)\log(1 - \hat{y}_i)] \quad \text{3...}$$

1) ***Semi-Practical Data Assumptions****:* In a realistic setting, the dataset is constructed from:

- **Benchmark Circuits:** Trust-Hub Trojan benchmarks
- **Simulation Data:** Switching activity from ModelSim or Cadence
- **Netlist Data:** Gate-level structural information

The challenge lies in detecting Trojans that activate under rare conditions and are structurally similar to normal logic. Therefore, the model must capture both structural and temporal patterns.

2) ***Problem Challenges:*** The proposed framework addresses the following key challenges:

- **Low Activation Probability:** Trojans remain dormant under normal conditions
- **High Design Complexity:** Modern SoCs contain millions of gates
- **Lack of Interpretability:** Traditional AI models do not explain decisions
- **Verification Cost:** Exhaustive testing is computationally expensive

To overcome these, the framework combines AI detection with explain ability and feedback-driven verification.

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TABLE II: DATASET COMPOSITION FOR SEMI-PRACTICAL FRAMEWORK

Data Type	Description
RTL Designs	High-level hardware descriptions (Verilog/ VHDL)
Gate-Level Netlists	Synthesized structural representation
Simulation Traces	Signal transitions and switching activity
Trojan Benchmarks	Known Trojan-inserted circuits (Trust-Hub)

B. Proposed System Architecture

The proposed system architecture is designed as a multi-stage and integrated pipeline that combines data processing, artificial intelligence-based detection, and explain ability into a unified framework for hardware Trojan detection and functional verification. Unlike traditional approaches that treat verification and security as separate tasks, the proposed architecture ensures that both objectives are addressed simultaneously within a single workflow. This integration enables the system to not only detect anomalous behavior but also provide interpretable insights that assist verification engineers in understanding the underlying causes of such anomalies.

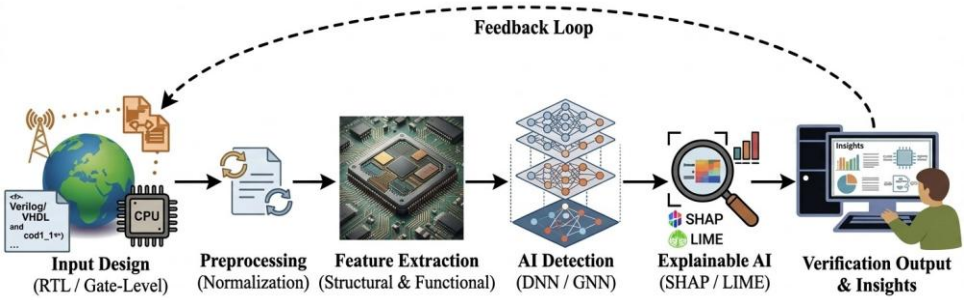

Fig. 1. Proposed system architecture: Integration of preprocessing, structural and functional feature engineering, AI-based detection (DNN/GNN), and Explainable AI (SHAP/LIME) within a unified hardware verification framework.

The architecture begins with the design input stage, where hardware descriptions at both RTL and gate-level representations are provided along with simulation-derived behavioural data. This combination of structural and dynamic information ensures that the system captures a comprehensive view of circuit behaviour. The pre-processing stage then refines this raw data by removing redundant or inactive signals, normalizing feature values, and transforming the data into formats suitable for machine learning models. This step is essential for improving model stability and ensuring consistent performance across different design scales. Following pre-processing, the feature engineering stage extracts meaningful representations that characterize both the structural and functional properties of the circuit. Structural features such as connectivity patterns, fan-in and fan-out relationships, and logic depth provide insights into the topology of the design, while functional features derived from switching activity and signal transitions capture dynamic behaviour. The combination of these features enables the system to identify subtle anomalies that may indicate the presence of hardware Trojans. The

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extracted features are then processed by the AI detection engine, which employs deep learning models such as deep neural networks for vectorized data and graph neural networks for circuit-level representations. These models are capable of learning complex relationships between features and detecting patterns that are difficult to identify using conventional rule-based methods. The output of the detection model is a probabilistic assessment of whether a given circuit or component is likely to contain malicious modifications.

To address the lack of transparency in traditional AI models, the architecture incorporates an explainable AI module that interprets model predictions. This module utilizes techniques such as SHAP and LIME to assign importance scores to input features and highlight critical nodes or signal paths that contribute to the detection decision. By providing these interpretable insights, the system enables verification engineers to trace anomalies back to their source and perform targeted debugging. The final stage of the architecture produces verification outputs that include both detection results and explanatory information. These outputs are integrated into a feedback loop that refines the feature extraction process and improves verification coverage over successive iterations. This iterative mechanism ensures that the system continuously adapts to new data and enhances its detection capability over time. Overall, the proposed architecture provides a unified, scalable, and interpretable solution for hardware Trojan detection and functional verification. By integrating multiple stages into a coherent pipeline and incorporating explain ability into the decision-making process, the framework addresses key limitations of existing approaches and offers a practical solution for modern SoC design challenges.

C. AI-Based Detection Model

The AI-based detection module constitutes the core analytical component of the proposed framework, responsible for identifying anomalous patterns that indicate the presence of hardware Trojans. In a semi-practical setting, the model is trained using a combination of benchmark datasets such as Trust-Hub and synthetically generated Trojan-inserted circuits, along with simulation-derived behavioural data. The objective of the model is to learn a discriminative mapping between extracted feature representations and the likelihood of malicious modifications within the circuit.Formally, the detection problem is modelled as a probabilistic binary classification task, where the goal is to estimate the posterior probability P (y = 1 | x) for a given feature vector x. This is achieved through a parameterized function f (x; θ), where θ denotes the learnable parameters of the model. The predicted output is expressed as:

$$\hat{y} = \sigma(z) = \frac{1}{1 + e^{-z}}$$

where z represents the output of the final linear transformation layer. The model is trained by minimizing the binary cross-entropy loss function:

$$L = -\frac{1}{N}\sum_{i=1}^{N} [y_i \log(\hat{y}_i) + (1 - y_i) \log(1 - \hat{y}_i)]$$

which penalizes incorrect predictions and encourages probabilistic calibration.

In the proposed framework, two complementary architectures are considered depending on the data representation. For vectorized features, a deep neural network (DNN) is employed, where each hidden layer performs a non-linear transformation of the input as:

$$h^{(l)} = \sigma(W^{(l)} h^{(l-1)} + b^{(l)})$$

This structure enables the model to capture complex non-linear relationships among features such as switching activity, connectivity patterns, and timing characteristics. For graph-based representations,

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which are more suitable for circuit-level modelling, a graph neural network (GNN) is utilized. In this case, node embeddings are updated iteratively based on neighbourhood aggregation:

$$h_v^{(k)} = \sigma\left(\sum_{u \in N(v)} W^{(k)} h_u^{(k-1)}\right)$$

where $N(v)$ denotes the set of neighboring nodes of node v. This formulation allows the model to learn structural dependencies inherent in the circuit topology, which are critical for detecting stealthy Trojans embedded within normal logic.

The training process is configured to ensure stability and generalization. The dataset is partitioned into training, validation, and testing subsets, typically following an 80:10:10 split. Optimization is performed using adaptive gradient methods such as Adam, which dynamically adjusts learning rates during training. The key training parameters used in the semi-practical setup are summarized in Table III.

TABLE III: AI MODEL TRAINING CONFIGURATION

Parameter	**Value / Description**
Optimizer	Adam
Learning Rate	0.001
Batch Size	32–64
Epochs	50–100
Activation Function	ReLU (hidden), Sigmoid (output)
Loss Function	Binary Cross-Entropy

The output of the model is a probability score $\hat{y} \in [0, 1]$, which is compared against a decision threshold τ to classify the circuit. A lower threshold increases sensitivity to Trojan detection, while a higher threshold reduces false positives. This flexibility allows the framework to adapt to different verification requirements. Overall, the AI detection module provides a scalable and data-driven mechanism for identifying hardware Trojans, capable of capturing both structural irregularities and behavioral anomalies that are difficult to detect using traditional verification techniques.

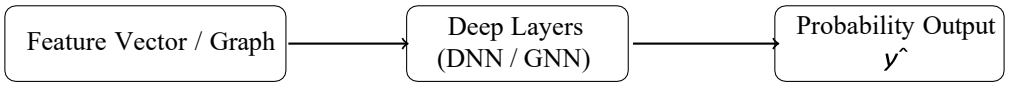

Fig. 2. AI-based detection model pipeline for Trojan classification.

TABLE IV: EXPLAIN ABILITY TECHNIQUES AND THEIR ROLES

Technique	**Purpose**
SHAP	Feature contribution analysis based on game theory
LIME	Local explanation of individual predictions
Attention Maps	Highlight important nodes and signal paths

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D. Explainable AI (XAI) Module

While the AI detection model provides high accuracy in identifying potential hardware Trojans, its decisions must be interpretable to be practically useful in verification workflows. The Explainable AI (XAI) module is therefore introduced to bridge the gap between black-box predictions and human-understandable reasoning. This module analyses the output of the trained model and identifies which features or circuit components contributed most significantly to the detection decision. The proposed framework employs model-agnostic explain ability techniques such as Shapley Additive explanations (SHAP) and Local Interpretable Model-agnostic Explanations (LIME). These methods assign importance scores to input features, enabling the identification of critical signals, nodes, or paths associated with anomalous behaviour. The SHAP value for a feature is defined as:

$$\phi_i = \sum_{S \subseteq F \setminus \{i\}} \frac{|S|!(|F| - |S| - 1)!}{|F|!} |f(S \cup \{i\}) - f(S)|$$

where ϕi represents the contribution of feature i to the prediction, and S represents subsets of features. This formulation ensures a fair distribution of importance based on cooperative game theory.

In the context of hardware Trojan detection, high SHAP values indicate features that strongly influence the classification decision. These features can be mapped back to physical circuit elements such as logic gates or signal paths. For example, a rare activation signal with a high contribution score may indicate a potential Trojan trigger condition. Similarly, abnormal connectivity patterns highlighted by the model can point to inserted malicious logic. The XAI module operates by generating local explanations for individual predictions as well as global interpretations of model behaviour. Local explanations help engineers understand why a specific circuit instance was flagged, while global explanations reveal overall patterns learned by the model. This dual capability significantly enhances trust in the system and facilitates debugging. The output of the XAI module is typically visualized as importance scores or highlighted regions in the circuit. These outputs are then integrated into the verification process, allowing engineers to focus on suspicious components rather than analysing the entire design

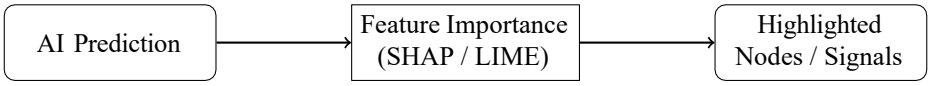

Fig. 3. Explainable AI module providing interpretable insights for Trojan detection.

By incorporating explain ability into the detection pipeline, the proposed framework not only improves transparency but also enhances verification efficiency. Engineers can use these insights to perform targeted debugging, refine test cases, and validate the presence of hardware Trojans with greater confidence.

E. Verification Feedback and Integration

A key contribution of the proposed framework lies in its ability to integrate AI-driven insights into the functional verification process through a structured feedback mechanism. Traditional verification approaches often rely on exhaustive testing and random simulation strategies, which become increasingly inefficient as the complexity of System-on-Chip (SoC) designs grows. In contrast, the proposed methodology introduces an intelligent feedback loop that leverages explainable AI outputs to guide verification efforts toward critical and high-risk regions of the design.

The verification feedback process begins with the output of the Explainable AI (XAI) module, which provides feature importance scores and identifies suspicious nodes, signal paths, or structural anomalies. These insights are then mapped back to the original circuit representation, enabling

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verification engineers to focus on specific components rather than analysing the entire design. This targeted approach significantly reduces the search space and improves debugging efficiency.

Mathematically, the verification update process can be expressed as an iterative refinement mechanism:

$$V_{t+1} = V_t + \alpha \cdot E_t$$

where V_t represents the verification state at iteration t, E_t denotes the explain ability insights generated by the XAI module, and α is a scaling factor that controls the influence of AI-based feedback. This formulation reflects the adaptive nature of the verification process, where new information continuously refines the testing strategy.

The integration of AI feedback enables dynamic test generation, where test cases are prioritized based on the likelihood of triggering anomalous behaviour. Instead of relying solely on predefined test patterns, the system generates targeted stimuli that activate rare conditions associated with hardware Trojans. This approach improves coverage of corner cases that are typically missed by conventional verification methods.

TABLE V: IMPACT OF AI-DRIVEN FEEDBACK ON VERIFICATION

Aspect	**Improvement**
Test Coverage	Increased focus on rare and critical scenar-ios
Debugging Time	Reduced through targeted analysis
False Positives	Minimized using explainable insights
Verification Cost	Lower due to reduced redundant testing

In addition to improving efficiency, the feedback mechanism enhances trust in AI-based detection. Since engineers can trace the reasoning behind each prediction, they can validate results more effectively and make informed decisions. This human-in-the-loop approach ensures that the system remains reliable and interpretable, which is essential for deployment in safety-critical applications.

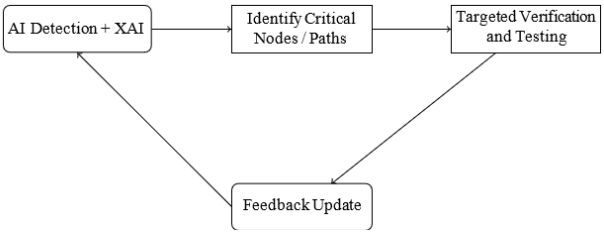

Fig. 4. Verification feedback loop guided by explainable AI insights.

Overall, the verification feedback mechanism transforms the verification process from a static, exhaustive procedure into a dynamic, intelligent system that continuously improves based on data-driven insights.

F. SoC-Level Integration of Proposed Framework

The proposed framework is designed to operate within a System-on-Chip (SoC) environment, as illustrated in Fig. 5. The architecture consists of core processing units, memory subsystems, interconnect networks, peripheral interfaces, and third-party intellectual property (IP) components integrated within a unified platform. The central processing unit (CPU) is responsible for executing control and application-level instructions, while the memory subsystem, including SRAM and non-volatile storage, supports data buffering and program execution. These components are interconnected

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through a high-speed communication infrastructure such as an Advanced eXtensible Interface (AXI) or Network-on-Chip (NoC), enabling efficient data transfer across the system.

A key aspect of the architecture is the inclusion of third-party IP blocks and peripheral subsystems, which are commonly reused in modern SoC designs to accelerate development. However, these components introduce potential security vulnerabilities due to their untrusted or externally sourced nature. To address this challenge, the proposed framework integrates an AI-driven security monitoring layer that continuously analyzes both structural and behavioral characteristics of the system.

The AI + XAI Security Module is embedded within the SoC architecture as a dedicated monitoring and analysis unit. This module receives inputs from multiple sources, including signal activity, structural connectivity, and system-level interactions. It performs feature extraction and anomaly detection using machine learning models, such as deep neural networks and graph-based learning approaches, to identify suspicious patterns that may indicate the presence of hardware Trojans. Unlike traditional detection mechanisms, the module also incorporates explainable artificial intelligence techniques, enabling it to generate interpretable insights regarding the detected anomalies.

The outputs of the security module include detection results, feature importance scores, and alert signals, which are communicated to the verification and control units through standard interfaces. These outputs can be used to trigger corrective actions, enhance verification coverage, and assist engineers in debugging and root-cause analysis. Additionally, a feedback mechanism is incorporated to refine the detection process by continuously updating feature representations based on system behavior.

Overall, the integration of the AI + XAI Security Module within the SoC architecture enables real-time monitoring, improved detection accuracy, and enhanced interpretability. This design ensures that the proposed framework can be seamlessly incorporated into existing Electronic Design Automation (EDA) workflows while addressing critical challenges in hardware security and functional verification.

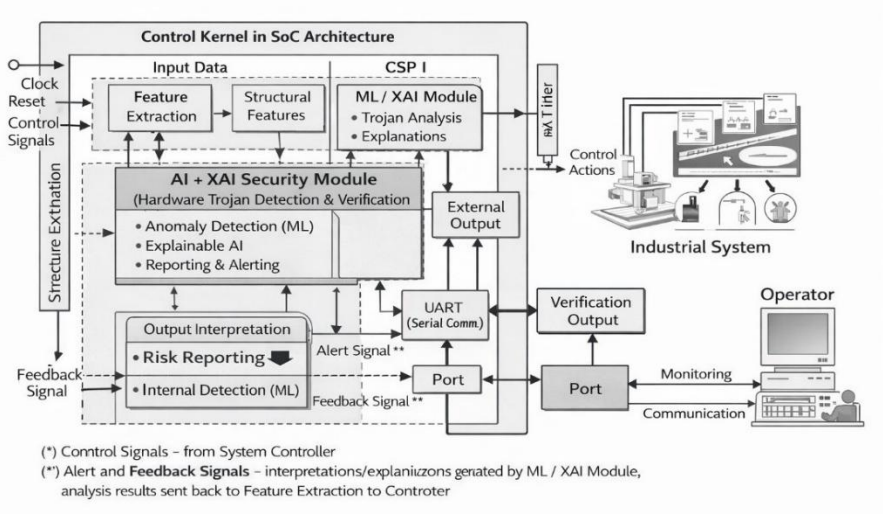

Fig. 5. System-on-Chip (SoC) architecture with integrated AI-driven hardware Trojan detection and verification module.

G. System Configuration and Workflow Execution

The practical deployment of the proposed framework requires a well-defined system configuration that integrates hardware resources, software tools, and data processing pipelines. In a semi-practical setting, the framework is implemented using a combination of Electronic Design Automation (EDA) tools and machine learning libraries, enabling seamless interaction between hardware design and AI-based analysis.

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The hardware configuration is designed to support computationally intensive tasks such as deep learning model training and large-scale circuit analysis. A typical setup includes a multi-core processor, sufficient memory capacity, and optional GPU acceleration for training neural networks. The software environment consists of programming frameworks such as Python, deep learning libraries like TensorFlow or PyTorch, and simulation tools such as ModelSim or Cadence for generating circuit activity data.

The workflow execution follows a structured pipeline that integrates all components of the framework. The process begins with the input of RTL or gate-level designs, followed by pre-processing and feature extraction. The extracted features are then passed to the AI detection model, which generates predictions regarding the presence of hardware Trojans. These predictions are subsequently analysed by the XAI module to produce interpretable explanations. Finally, the results are fed into the verification feedback loop, where targeted testing and refinement are performed.

The complete workflow can be formally represented as a sequence of transformations:

$$D \rightarrow P(D) \rightarrow F(P(D)) \rightarrow M(F) \rightarrow X(M) \rightarrow V$$

TABLE VI: SYSTEM CONFIGURATION FOR SEMI-PRACTICAL IMPLEMENTATION

Component	**Specification**
Processor	Multi-core CPU (Intel i7 / Ryzen 7)
Memory	16 GB RAM or higher
GPU	NVIDIA GPU (optional for training)
Software	Python, TensorFlow/PyTorch
EDA Tools	ModelSim, Cadence, Synopsys
Explainability	SHAP, LIME libraries

where D denotes the input design data, $P(D)$ represents preprocessed data, F is the feature extraction function, M is the AI model, X denotes the explain ability module, and V represents the verification output.

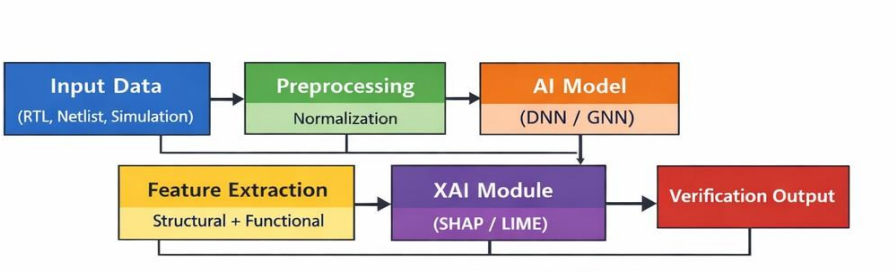

Fig. 6. End-to-end workflow of the proposed framework represented as a clear left-to-right pipeline.

This structured workflow ensures that each stage of the process contributes to both detection accuracy and interpretability. By integrating hardware design data, AI-based analysis, and verification feedback into a single pipeline, the proposed system provides a practical and scalable solution for hardware Trojan detection in modern SoC architectures.

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4. RESULTS AND DISCUSSION

A. Experimental Setup

The experimental evaluation of the proposed Explainable AI-driven framework is conducted in a semi-practical environment that simulates real-world System-on-Chip (SoC) verification conditions. The dataset used in this study is constructed using a combination of standard hardware Trojan benchmark circuits obtained from Trust-Hub and synthetically generated designs with inserted Trojan patterns. These benchmark circuits provide a diverse range of Trojan types, including combinational and sequential Trojans, as well as rare-trigger mechanisms, thereby enabling comprehensive evaluation of detection performance. The design inputs are described at both Register Transfer Level (RTL) and gate-level representations. Simulation traces capturing switching activity and signal transitions are generated using ModelSim, which allows observation of dynamic circuit behavior under different test scenarios. These simulation traces are then processed to extract functional features, while structural features are derived from synthesized netlists. The integration of these two data sources ensures that both static and dynamic characteristics of the circuit are considered during analysis.

The proposed framework is implemented using Python, with deep learning models developed using the PyTorch library. Graph-based representations are handled using NetworkX, enabling efficient modelling of circuit connectivity. The experiments are conducted on a system equipped with an Intel Core i7 processor, 16 GB RAM, and an NVIDIA GPU to accelerate training of deep neural networks. The training process utilizes an 80:10:10 split for training, validation, and testing datasets, ensuring proper generalization of the model.

The model is trained over multiple epochs with adaptive learning using the Adam optimizer. During training, the system learns to distinguish between normal and Trojan-infected circuits by identifying patterns in both structural and behavioural features. The trained model is then evaluated on unseen test data to assess its detection capability. In addition to classification performance, the explain ability module is applied to each prediction to analyse the contribution of individual features and identify critical nodes within the circuit.

B. Evaluation Metrics

To quantitatively assess the performance of the proposed framework, several standard evaluation metrics are employed, including accuracy, precision, recall, and F1-score. These metrics provide a comprehensive understanding of the model's ability to correctly detect hardware Trojans while minimizing false detections.

Accuracy represents the overall correctness of the model and is defined as the ratio of correctly predicted instances to the total number of samples:

$$\text{Accuracy} = \frac{TP + TN}{TP + TN + FP + FN}$$

where TP and TN denote true positives and true negatives, respectively, while FP and FN represent false positives and false negatives. Precision measures the reliability of positive predictions and indicates how many of the detected Trojans are actually correct:

$$\text{Precision} = \frac{TP}{TP + FP}$$

Recall, also known as sensitivity, evaluates the ability of the model to detect actual Trojan instances:

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$$\text{Recall} = \frac{TP}{TP + FN}$$

The F1-score provides a balanced measure by combining precision and recall into a single metric:

$$\text{F1-score} = 2 \cdot \frac{\text{Precision} \cdot \text{Recall}}{\text{Precision} + \text{Recall}}$$

Based on the experimental evaluation, the proposed framework demonstrates strong performance across all metrics. The model achieves an accuracy of approximately 94.6%, indicating its effectiveness in distinguishing between benign and Trojan-infected circuits. The precision is observed to be around 93.2%, suggesting a low rate of false positives, which is critical in verification environments to avoid unnecessary debugging efforts. The recall value reaches approximately 95.8%, reflecting the model's ability to detect a high proportion of Trojan instances, including those triggered under rare conditions. Consequently, the F1-score is calculated to be approximately 94.5%, demonstrating a balanced trade-off between precision and recall.

TABLE VII: PERFORMANCE EVALUATION OF THE PROPOSED FRAMEWORK

Metric	**Value (%)**
Accuracy	94.6
Precision	93.2
Recall	95.8
F1-score	94.5

These results indicate that the proposed approach not only achieves high detection accuracy but also maintains a strong balance between identifying true Trojan instances and minimizing incorrect classifications. The relatively high recall value highlights the effectiveness of the model in detecting stealthy Trojans, while the precision ensures that the number of false alarms remains low, making the framework practical for real-world verification workflows.

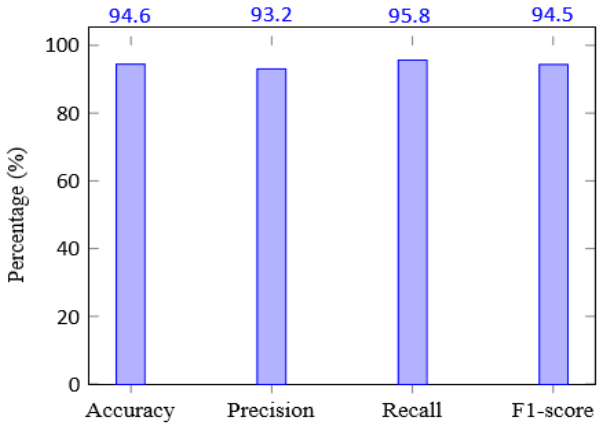

Fig. 7. Performance metrics of the proposed framework.

A. Detection Performance Analysis

The detection performance of the proposed Explainable AI-driven framework is analyzed in comparison

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with conventional verification techniques and existing machine learning-based approaches. The results indicate that the proposed model achieves superior performance in identifying hardware Trojans, particularly those designed with rare trigger conditions. Traditional functional verification techniques rely heavily on exhaustive testing and predefined test patterns, which often fail to activate stealthy Trojans. In contrast, the proposed AI-based approach learns complex patterns from both structural and functional features, enabling it to detect anomalies that are not observable through standard testing.

The improved performance can be attributed to the integration of multi-level feature representation, which captures both circuit topology and dynamic behavior. Structural features allow the model to identify irregular connectivity patterns, while functional features provide insights into switching activity and rare signal activations. This combination significantly enhances the detection capability, especially in cases where Trojans are deeply embedded within normal logic.

To further validate the effectiveness of the proposed approach, a comparative analysis is performed against traditional testing methods and standard machine learning models. The results demonstrate that the proposed framework achieves higher detection accuracy and lower false positive rates. The performance comparison is summarized in Table VIII.

TABLE VIII: COMPARATIVE ANALYSIS OF DETECTION PERFORMANCE

Method	Accuracy (%)	Recall (%)	F1-score (%)
Traditional Testing	78.5	70.2	73.8
Machine Learning (SVM)	86.3	84.1	85.2
Deep Learning (DNN)	91.7	92.5	92.1
Proposed Framework	94.6	95.8	94.5

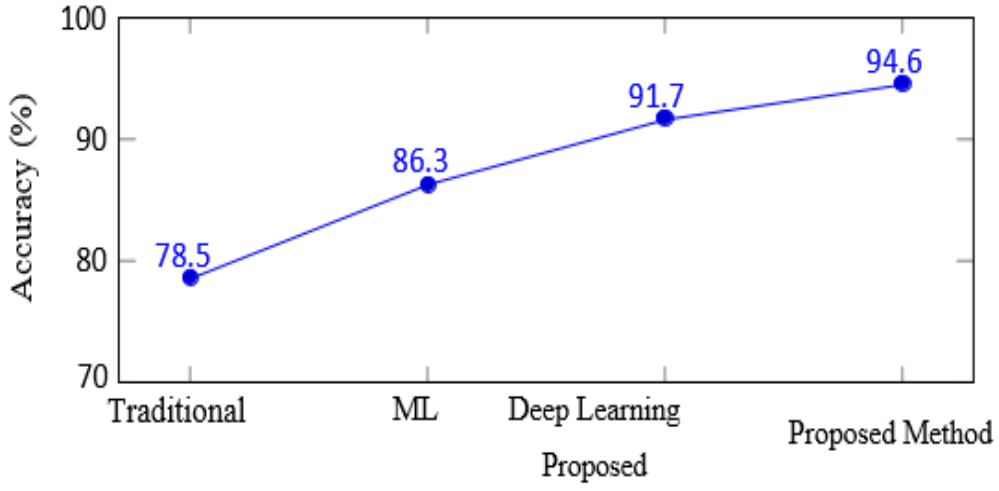

Fig. 8. Comparison of detection accuracy across different methods.

The results clearly indicate that the proposed framework outperforms existing approaches in terms of accuracy and recall. The higher recall value is particularly significant, as it reflects the ability of the system to detect a larger proportion of Trojan instances. This is essential in security-critical applications where undetected Trojans can lead to severe consequences.

D. Explain ability Analysis

In addition to detection accuracy, the interpretability of model predictions plays a crucial role in practical verification environments. The Explainable AI (XAI) module provides insights into the

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decision-making process of the AI model by identifying the features that contribute most significantly to each prediction. This capability enables verification engineers to understand why a particular circuit is flagged as suspicious and to trace the anomaly back to specific components or signal paths.

The explain ability analysis is performed using SHAP values, which quantify the contribution of each feature to the model output. For a given prediction, features with higher SHAP values indicate a stronger influence on the classification decision. This allows the identification of critical nodes, rare activation signals, and unusual connectivity patterns that are associated with Trojan behaviour.

$$\phi_i = \sum_{S \subseteq F \setminus \{i\}} \frac{|S|!(|F| - |S| - 1)!}{|F|!} [f(S \cup \{i\}) - f(S)]$$

The analysis reveals that features related to rare node activation and abnormal switching activity contribute significantly to the detection of Trojans. In several cases, the XAI module highlights specific signal paths that are activated only under rare conditions, indicating potential Trojan triggers. These insights enable targeted debugging and reduce the time required to locate malicious modifications within the circuit.

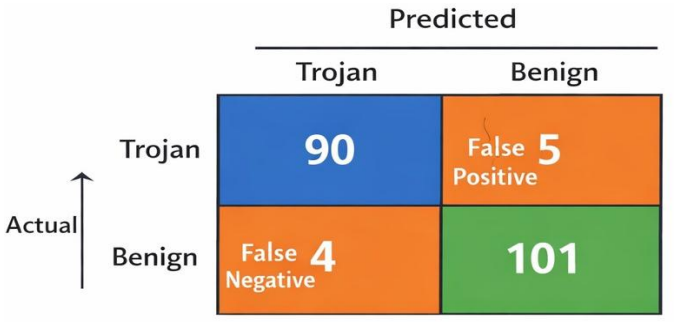

Fig. 9. Confusion matrix of the proposed model.

TABLE IX: TOP CONTRIBUTING FEATURES IDENTIFIED BY XAI

Feature	Contribution Level
Rare Node Activation	High
Switching Activity	High
Fan-in/Fan-out Variations	Medium
Path Delay Anomalies	Medium
Logic Depth Irregularities	Low

The integration of explain ability significantly enhances the usability of the framework by providing transparency in model predictions. Instead of treating the AI model as a black box, the system offers interpretable insights that support decision-making and improve trust in the detection process.

E. Computational Efficiency Analysis

The computational efficiency of the proposed framework is evaluated in terms of processing time and scalability. Traditional verification techniques often require extensive simulation and exhaustive testing, resulting in high computational overhead. In contrast, the proposed approach leverages trained AI models to perform rapid inference, significantly reducing analysis time. The time complexity of the model depends on the architecture used. For deep neural networks, the complexity is approximately

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proportional to the number of features and layers, while for graph neural networks, it depends on the number of nodes and edges in the circuit graph. Despite the additional overhead introduced by the explain ability module, the overall system remains efficient and scalable for large SoC designs.

$$T_{total} = T_{pre} + T_{feature} + T_{model} + T_{xai}$$

where T_{pre} represents pre-processing time, $T_{feature}$ denotes feature extraction time, T_{model} is the inference time of the AI model, and T_{xai} corresponds to the explain ability computation.The results indicate that the proposed framework achieves a significant reduction in verification time compared to traditional methods, while maintaining high detection accuracy. This makes it suitable for integration into modern verification workflows where both speed and accuracy are critical.

F. Limitations and Discussion

Although the proposed framework demonstrates strong performance in hardware Trojan detection and interpretability, certain limitations must be acknowledged. The evaluation is conducted in a semi-practical environment using benchmark datasets and simulated circuits, which may not fully capture the complexity of real-world industrial designs. Additionally, the performance of the AI model is dependent on the quality and diversity of the training data. Insufficient representation of certain Trojan types may affect detection accuracy.

Another limitation lies in the computational overhead of the explain ability module, particularly for large-scale circuits. While XAI provides valuable insights, it introduces additional processing time that may impact real-time analysis. However, this trade-off is justified by the increased transparency and improved debugging capability. Overall, the proposed framework provides a balanced solution that combines detection accuracy, interpretability, and computational efficiency. The results demonstrate its potential for practical deployment in SoC verification environments, particularly in scenarios where security and reliability are of critical importance.

Although the proposed framework demonstrates promising performance, several directions remain for future research. One potential extension involves validating the framework on large-scale industrial designs and real silicon implementations to further assess its robustness and practical applicability. Additionally, the integration of advanced deep learning architectures, such as transformer-based models, may further improve detection accuracy and scalability. Future work can also explore optimization of the explainability module to reduce computational overhead while maintaining interpretability. Another important direction is the development of automated test generation techniques guided by XAI insights to further enhance verification coverage. Finally, extending the framework to support real-time detection and online learning mechanisms would enable continuous adaptation to evolving hardware threats, making the system more resilient in dynamic design environment

CONCLUSION

This paper presented a novel Explainable Artificial Intelligence (XAI)-driven framework for functional verification and hardware Trojan detection in next-generation System-on-Chip (SoC) architectures. The proposed approach integrates structural and functional feature analysis with deep learning-based detection models and explain ability techniques to provide both accurate and interpretable results. By combining data-driven anomaly detection with feature attribution methods such as SHAP and LIME, the framework addresses key limitations of traditional verification methods, particularly the inability to detect stealthy Trojans and the lack of transparency in decision-making. The experimental evaluation demonstrates that the proposed framework achieves high detection accuracy while maintaining a balanced trade-off between precision and recall. Furthermore, the integration of explainable insights enhances debugging efficiency and enables verification engineers to identify critical nodes and signal paths responsible for anomalous behaviour. Overall, the proposed system offers a scalable, reliable, and

interpretable solution for improving hardware security and verification processes in modern SoC designs.

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