Journal of Information Systems Engineering and Management
2025, 10(21s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

Single-Phase Five Level Modified Neutral Point Clamped Grid-Tied Inverter Topology with a Front-End Multilevel Boost Converter

Y Sravan kumar[1], T Murali Krishna[2], G Yesuratnam[3]

1 Research Scholar, Department of Electrical Engineering, University college of Engineering, Osmania University, Hyderabad, Telangana, India.

2Associate Professor, Department of Electrical and Electronics Engineering, Chaitanya Bharathi Institute of Technology, Hyderabad, Telangana, India.

3 Senior Professor, Department of Electrical Engineering, University college of Engineering, Osmania University, Hyderabad, Telangana, India.

ARTICLE INFO

Received: 16 Dec 2024

Revised: 01 Feb 2025

Accepted: 16 Feb 2025

ABSTRACT

Traditionally, the standalone performance of a single-phase fault-tolerant five-level neutral-point-clamped inverter (5L-NPC), powered by two rigid direct current (DC) sources, has been examined with an emphasis on the level shifted pulse width modulation (LS-PWM) method. In this configuration, the bidirectional switch setup incorporates four diodes and a single IGBT switch, which inherently leads to higher conduction losses in the system. Typically, NPC inverter topologies face challenges related to the balancing of DC-link capacitor voltages (DCL-CVs). In recent studies, researchers have addressed the front-end voltage balancing challenge by employing a dedicated control strategy, which necessitates the use of voltage sensors for implementation. This research presents an advancement in single-phase grid integration using a modified five-level neutral point clamped (M5L-NPC) inverter topology, addressing the previously mentioned issues. In this configuration, a front-end multilevel boost converter (FE-MLBC) is employed to autonomously balance the DCL-CVs while achieving voltage boosting with a reduced duty cycle. This paper discusses the operation of the M5L-NPC topology in both standalone and grid-connected modes, including the self-regulation of DCL-CVs. The grid-connected system's key objectives, such as reactive power control (RPC), active power control (APC), and the injection of sinusoidal current with minimal harmonic distortion, are comprehensively analyzed using a straightforward simple proportional resonant (PR) based control approach

Keywords: grid-tied inverter, pulse width modulation, multilevel boost converter, proportional resonant, harmonic distortion.

I. INTRODUCTION

Power electronics play a crucial role in integrating renewable energy sources (RESs) with the grid, with multilevel inverters (MLIs) emerging as essential components for efficiently harnessing energy from RESs and improving power quality [1]. MLIs have emerged as a significant area of research in the field of energy conversion, particularly in the modern era. Their widespread adoption, efficient performance, and versatility have made them integral to different power applications. Their application in advanced and diverse fields have been demonstrated as potential innovative solutions to numerous challenges [2].

By employing various PWM techniques in real-time and integrating fast closed-loop control algorithms, researchers can accurately and dynamically regulate the output voltages of MLIs to meet grid requirements and minimize harmonic distortion [3]. This research can improve the efficiency and reliability of grid-connected MLI systems, enhancing their effectiveness in renewable energy integration, grid stabilization, and industrial power applications [4].

A review of existing studies highlights a consistent correlation between switching frequency and

power density, where increasing PWM frequencies shifts the harmonic spectrum of a power electronic converter's output voltage and current to higher frequencies, ultimately allowing for a reduction in harmonic filter size [5]. The decision to use either high or low switching frequencies in power electronic converters has a substantial impact on power quality, the size of filters, and overall system efficiency [6].

A higher switching frequency allows for the implementation of smaller passive harmonic filters [7]. However, in the absence of such filters, increased switching frequency can lead to greater distortions in the inverter's output voltage [8]. These findings may appear contradictory, especially given the current trend of adopting higher switching frequencies to reduce the size of magnetic components [9].

With the increasing adoption of renewable energy, five-level MLI-based photovoltaic (PV) systems have become essential due to their superior efficiency, lower harmonic distortion, and enhanced power quality compared to conventional designs. The control strategy for MLIs generally consists of three main stages: reference generation, modulation, and gate signal generation [10].

In the reference generation stage, the desired voltage waveform and corresponding levels are determined. Modulation methods, such as PWM, then convert these references into appropriate switching sequences. Lastly, the gate signal generation stage produces accurately timed signals to control the inverter's semiconductor switches [11, 12]. Effective synchronization of these stages is crucial for optimal MLI performance, ensuring high-quality output waveforms, reduced harmonic distortion, and improved energy efficiency, particularly in solar power applications [13].

A single-phase five-level fault-tolerant inverter topology designed for standalone PV systems using dual rigid DC sources [14]. While the study highlights advancements in partial fault tolerance for off-grid operation, the proposed architecture exhibits limitations in achieving full fault-tolerant capabilities and lacks adaptability for seamless integration with grid-connected applications due to its structural and operational constraints [15].

In 5L-NPC inverter architectures, achieving effective dc-link capacitor voltage balancing and meticulous design optimization are critical prerequisites to ensure operational stability and performance integrity prior to deployment in grid-connected systems [16]. In scholarly investigations addressing static synchronous compensator (STATCOM) systems, capacitor voltage balancing in dc-link configurations has been analyzed using chopper circuit topologies [17].

Technical analyses further extend to M5L-NPC inverters, emphasizing capacitor equalization strategies and grid synchronization methodologies to enhance operational reliability and performance in grid-integrated environments [18]. The existing front-end power stage in this configuration inherently lacks voltage amplification functionality and necessitates the incorporation of auxiliary voltage monitoring components, thereby introducing design complexity and limiting its adaptability in applications requiring dynamic voltage regulation.

Conventional boost converter topologies are predominantly employed in existing systems to achieve front-end voltage amplification [19]. However, such architectures exhibit inherent limitations in scalability for integration into multilevel dc-link frameworks and introduce operational inefficiencies due to their dependency on elevated duty cycle ratios, thereby restricting their practicality in advanced power conversion systems [20].

Recent studies have introduced innovative topologies for multilevel voltage boosting architectures with integrated self-regulating dc-link capacitor voltage balancing mechanisms [21, 22]. These advancements demonstrate the capability to achieve stable multilevel output waveforms while operating at reduced duty cycle ratios, overcoming traditional limitations in conventional boost-based systems and enhancing operational efficacy in high-efficiency power conversion applications [23, 24].

This study advances prior research by integrating a MLBC architecture with a PR control scheme for single-phase grid synchronization of M5L-NPC inverter topology. The proposed framework achieves inherent capacitor voltage balancing without auxiliary control mechanisms and enables voltage amplification at reduced duty cycles, thereby enhancing operational efficiency and simplifying system design in grid-connected power conversion systems.

The manuscript is structured as follows: Section 2 delineates the circuit architecture, operational principles, and analytical framework of the proposed M5L-NPC grid-tied inverter (GTI) topology coupled with a FE-MLBC. Section 3 evaluates the system's performance through rigorous numerical

simulation studies, accompanied by detailed discussions on steady-state and transient behavior under diverse operational scenarios. The concluding section synthesizes key findings, underscores the technological contributions of the proposed topology, and discusses broader implications for advanced power conversion systems in renewable energy integration and grid-stability applications.

II. CIRCUIT DESIGN AND ANALYSIS OF A NOVEL M5L-NPC GTI TOPOLOGY INTEGRATED WITH A FE-MLBC

Brief Circuit Description of FE-MLBC

Existing literature predominantly investigates the standalone operational configurations of the 5L-NPC inverter topology [14]. However, conventional implementations necessitate dual DC input sources and employ bidirectional switching modules incorporating four diodes, inherently contributing to elevated conduction losses. Furthermore, prior contributions have not rigorously addressed the critical challenge of front-end voltage balancing, leaving a significant gap in the analysis of this topology's grid-integration capabilities.

While [18] delineates a chopper-based circuitry for front-end voltage stabilization and grid synchronization, the proposed architecture necessitates supplementary voltage sensing modules, dedicated control algorithms, and lacks inherent voltage-boosting functionality, thereby restricting its applicability in dynamic grid-interactive scenarios.

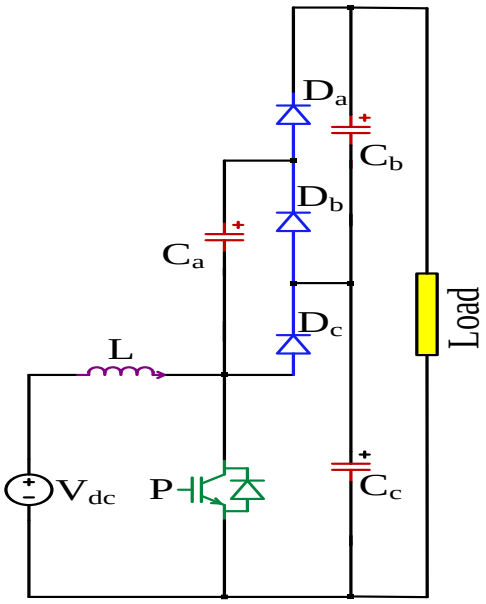


Fig.1 Circuit diagram of MLBC

This work employs a transformer less MLBC [21] operational framework to achieve voltage amplification and autonomous stabilization of front-end DCL-CVs, resolving inherent imbalance challenges while enhancing power conversion efficacy. The circuit configuration of the MLBC, illustrated in Fig. 1, comprises a single inductor, three capacitors, three diodes, and one actively controlled switch.

This topology offers a voltage gain of $\frac{2}{1-n}$, minimizes switch voltage stress, and inherently balances the DC-link CVs.

The MLBC integrates the principles of both boost conversion and switched-capacitor techniques. It ensures a continuous input current, supports unidirectional current flow, and operates efficiently at high switching frequencies.

Additionally, its modular design allows for seamless expansion by incorporating additional levels without altering the core circuit structure. When the duty cycle is set to D=0.5, the converter operates within its linear region, ensuring optimal performance.

Building on the MLBC framework, this paper proposes an extended M5L-NPC topology for single-phase grid integration, with the conceptual architecture illustrated in Fig. 2. The MLBC front-end first stage inherently self-balances DCL-CVs under a fixed 50% duty cycle (D = 0.5), while simultaneously enabling intrinsic voltage-boosting functionality without auxiliary circuitry. In the second stage, the 5L-NPC inverter is interfaced with the grid via an inductor filter. This inverter configuration comprises six insulated-gate bipolar transistor (IGBT) switches, a bidirectional switch, and two discrete diodes.

The present study extends the topology introduced in [18], incorporating modifications to the front-end stage to enhance system performance. The topology generates five discrete voltage levels across VAB: 0 Vdc (switches: I_2, I_3, I_5), +0.5 Vdc (I_1, I_2, I_5), +1 Vdc (I_1, I_2, I_7), -0.5 Vdc (I_2, I_3, I_6), and -1 Vdc (I_3, I_4, I_6), with each level corresponding to a unique combination of conducting switches.

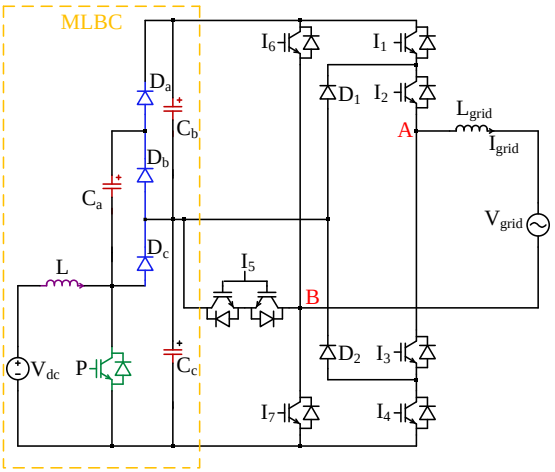


Fig.2 Circuit diagram of proposed 1-phase M5L-NPC grid-tied Inverter (GTI) with FE-MLBC

RESULTS AND DISCUSSIONS

Standalone Mode: R and RL-Loads:

Prior to transitioning to a 1-phase grid-connected configuration, the dynamic operational characteristics of the proposed topology (illustrated in Fig. 2) were rigorously evaluated in an autonomous operational regime. Under this standalone validation framework, two distinct load configurations—a purely resistive (R) load and a composite resistive-inductive (RL) load—were systematically examined to assess the system's transient and steady-state behavior.

The corresponding simulation parameters, meticulously calibrated to reflect realistic operational scenarios, are comprehensively delineated in Table 1. This preliminary analysis ensured robust validation of the topology's stability and performance fidelity under varying load conditions prior to grid integration.

Table 1 Standalone mode: Parameter values

S. No	Parameter	Value
1.	R-Load	41.95Ω
2.	L-Load	40mH
3.	Fsw	10kHz
4.	Vdc	100V
5.	Ca	4700µF
6.	Cb	4700µF
7.	Cc	4700µF
8.	Duty-P	0.5
9.	L	1mH

In power electronic systems, the selection and implementation of an appropriate control strategy serves as a critical determinant of operational efficacy. For the proposed topology, a two-stage methodological approach has been adopted. Initially, the MLBC stage employs a fixed 50% duty cycle

for switch-P, establishing a foundational operational regime. Subsequently, the inverter stage integrates an advanced unipolar phase disposition pulse-width modulation (UPD-PWM) technique, a strategic departure from conventional phase-disposition methods.

This UPD-PWM architecture, illustrated in Fig. 3, utilizes two interleaved triangular carrier signals and a logic-based modulation scheme to synthesize a five-level output voltage waveform. Notably, this technique minimizes carrier signal requirements, thereby streamlining the control framework and reducing computational overhead compared to traditional multilevel PWM strategies.

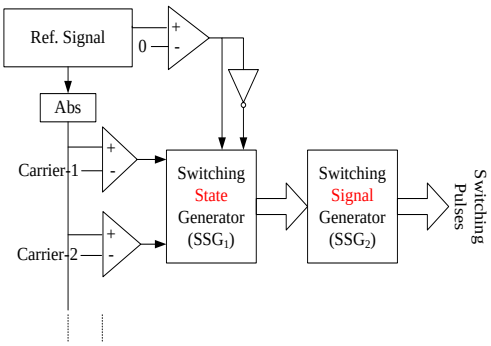
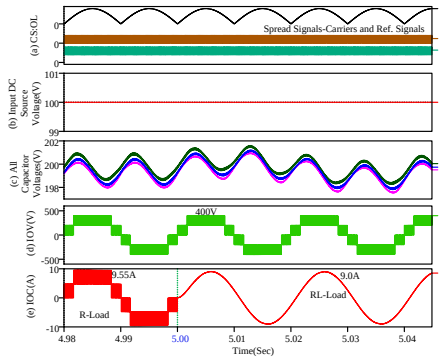


Fig.3 Block diagram of UPD-PWM Technique-M5L-NPC topology

Concurrently, the MLBC stage demonstrates an intrinsic self-balancing capability for DC-link capacitor voltages (CVs), eliminating the need for sensor-based feedback mechanisms or auxiliary control loops. This autonomous voltage regulation enhances the topology's operational efficiency while simplifying system architecture. Furthermore, the MLBC configuration achieves a voltage amplification ratio of 4:1, elevating the output (total DC-link voltage) to 400V from an input voltage of Vdc=100 V. This synergistic integration of simplified PWM modulation and self-stabilizing DC-link dynamics underscores the topology's adaptability and robustness in high-gain, low-complexity applications.

Fig. 4 presents the transient state analysis (TSA) of a step load transition from resistive (R) to resistive-inductive (RL) under a fixed modulation index (MI) of 0.99. Subfigure (a) depicts the open-loop control architecture, illustrating the system's operational framework during dynamic adjustments. Subfigure (b) highlights the stability of the input DC source, maintaining a constant magnitude of 100 V throughout the transient event. Subfigure (c) demonstrates the autonomous voltage balancing capabilities of the capacitors, each converging to a steady-state value of 200 V despite load perturbations. Subfigure (d) reveals the inverter output voltage (IOV) waveform, achieving a symmetrical peak amplitude of ±400 V, consistent with the system's designed voltage amplification. Finally, subfigure (e) captures the transient response of the inverter output current (IOC), exhibiting a peak reduction from 9.55 A to 9.0 A post the load transition at t=5 s, thereby validating the controller's efficacy in managing dynamic load variations while preserving operational stability. This comprehensive analysis underscores the system's robustness in maintaining performance metrics under abrupt load changes.



4 Step Change of Load at t=5sec (R to RL-Load) with MI=0.99: Results

Fig. 5 illustrates the TSA of a step load transition from R to RL under a dynamic MI shift from 0.6 to 0.99 at t=5 s. Subfigure (a) outlines the open-loop control scheme, emphasizing the absence of feedback mechanisms during the system's operational response. Subfigure (b) confirms the input DC source's stability, sustaining a consistent voltage magnitude of 100 V despite simultaneous load and MI variations. Subfigure (c) highlights the inherent self-balancing behavior of all capacitors, which stabilize autonomously at 200 V, showcasing robust voltage regulation independent of control-loop dynamics.

Subfigure (d) displays the IOV, maintaining a peak amplitude of ±400 V, indicative of the topology's inherent voltage-boosting capability under varying modulation indices. Subfigure (e) captures the transient evolution of the IOC, where the peak magnitude decreases from 9.5 A to 9.0 A post t=5 s, reflecting the combined influence of MI escalation and load impedance alteration. This analysis underscores the system's intrinsic stability and adaptability in open-loop configurations, even during concurrent modulation and load transients, while preserving critical operational parameters within design specifications.

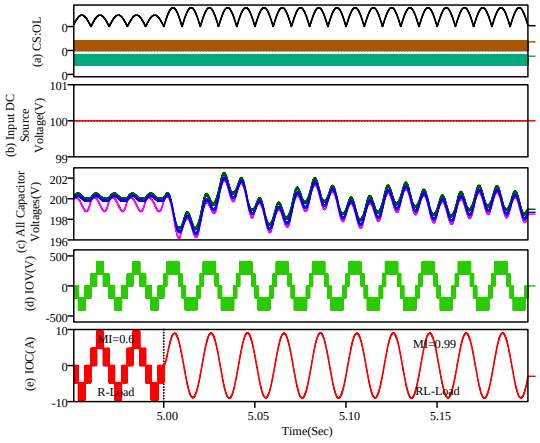


Fig.5 Step Change of Load at t=5sec (R to RL-Load) with MI=0.6 to 0.99: Results

Fig.6 presents an open-loop (OL) control scheme analysis, focusing on the operational stresses of critical power semiconductor components. Subfigure (a) characterizes the voltage stress across switch-P, revealing a peak magnitude of 200 V, equivalent to half the nominal output voltage ($V_0/2$), which aligns with the theoretical voltage distribution of the topology.

Subfigure (b) quantifies the current stress of switch-P, demonstrating a peak amplitude of 40 A. These results collectively validate the switch's operational robustness under OL control, as the observed stresses remain within safe operating limits despite the absence of feedback mechanisms.

The analysis underscores the inherent electrical behavior of the converter architecture, emphasizing its suitability for applications requiring simplified control frameworks while maintaining device integrity and performance consistency with theoretical designexpectation

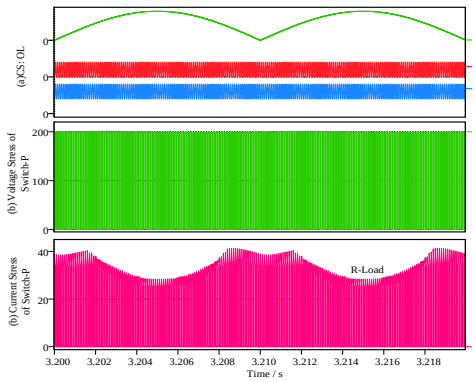


Fig.6 Voltage and Current Stress of Switch-P: Results

Grid-Tied Inverter (GTI) Mode: Results

The simulation parameters for GTI operation are detailed in Table 2. While prior research [18] employed a conventional PI controller preceding the PWM stage to regulate grid current injection, this approach exhibited limitations in achieving precise tracking of the grid's peak current reference.

To address these challenges, the present study proposes a proportional-resonant (PR) control strategy, which demonstrates enhanced performance in harmonic compensation and reference tracking compared to the PI-based methodology. The architecture of the PR control system is illustrated in Fig. 7. Subsequent implementation of this advanced control strategy within the framework of Fig. 2 yields significant improvements in current regulation accuracy and dynamic response, as evidenced by the results.

. Table 2 GTI Operation: Parameter Values

S. No	Parameter	Value
1.	Power Rating	2kVA
2.	Vdc	100V
3.	Vgrid	230V,50Hz
4.	Fsw	10kHz
5.	L-filter	13.56mH
6.	Ca	4700µF
7.	Cb	4700µF
8.	Cc	4700µF
9.	Duty-P	0.5
10.	L	1mH

Subfigure (c) depicts the five-level IOV waveform, retaining its peak amplitude of ±400 V during the transition. Subfigure (d) captures the dynamic shift from lagging PF to UPF, validating the PR-based control scheme's efficacy in concurrently regulating RPC and APC. These results underscore the system's robust dynamic performance, harmonic resilience, and seamless power factor correction capabilities under transient load scenarios.

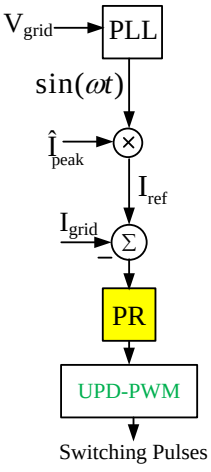


Fig.7 PR-based control strategy: GTI Operation

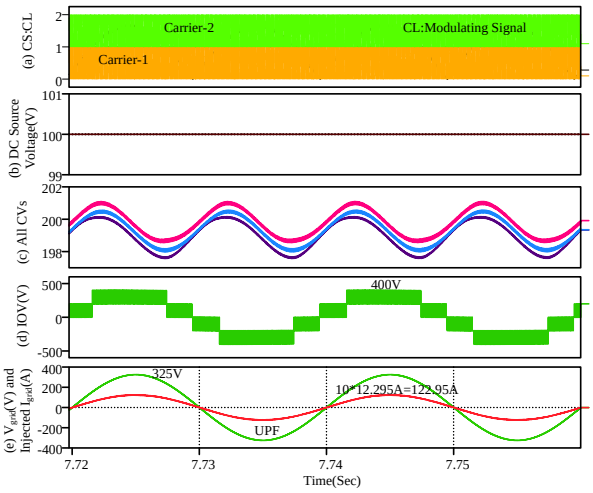


Fig.8 SSA results under UPF mode: GTI Operation

Fig. 8 presents the steady-state analysis (SSA) under UPF operation, with the grid current reference peak regulated to 12.295 A. Subfigure (a) illustrates the reference and carrier signal waveforms within the grid's closed-loop control architecture. Subfigure (b) displays the input DC source voltage, maintained at 100 V, while subfigure (c) confirms balanced DC-link CVs stabilized at 200 V.

Subfigure (d) demonstrates the five-level IOV waveform, exhibiting a peak magnitude of ±400 V. Subfigure (e) highlights the UPF operation, validating effective APC with a maximum active power output of 2 kW. These results collectively underscore the system's capability to maintain precise voltage regulation, harmonic suppression, and power quality under steady-state conditions.

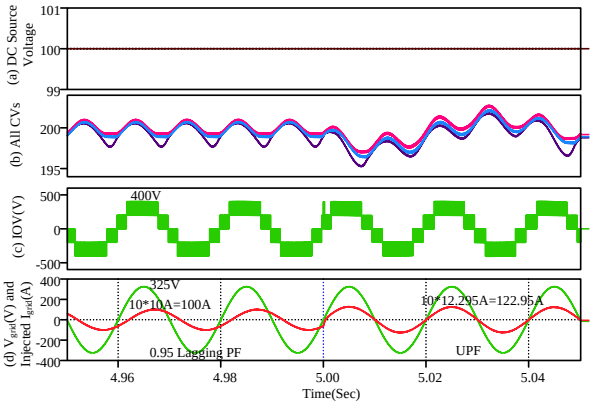


Fig.9 TSA results (0.95 lagging PF to UPF at t=5sec): GTI Operation

Fig. 9 illustrates the transient-state analysis (TSA) under a step change in power factor (PF) from 0.95 lagging to UPF at t = 5 s, accompanied by a step adjustment in the reference peak injected grid current from 10 A to 12.295 A. Subfigure (a) displays the input DC source voltage profile, maintained at a constant Vdc= 100 V throughout the transient. Subfigure (b) confirms the balanced DC-link CVs, stabilized at 200 V despite the dynamic operating conditions

Subfigure (d) captures the system's response to the lagging-to-leading PF transition, validating the PR-control strategy's capability to seamlessly govern both inductive and capacitive RPC while sustaining precise grid current regulation. These results underscore the controller's versatility in managing bidirectional power factor adjustments, ensuring voltage stability, harmonic attenuation, and robust dynamic performance under complex grid-reactive load interactions.

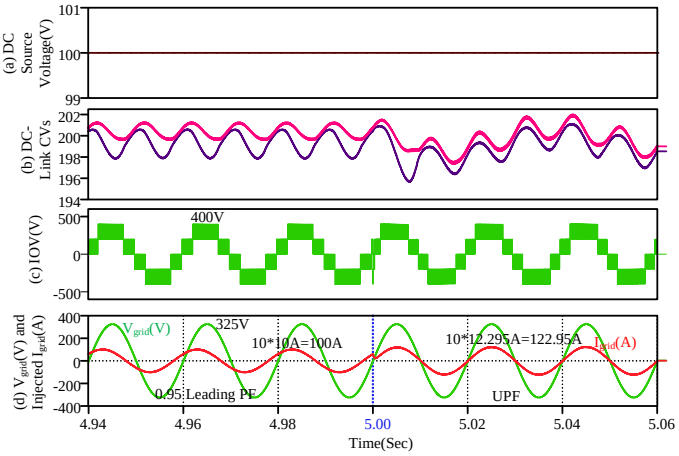


Fig.10 TSA results (0.95 leading PF to UPF at t=5sec): GTI Operation

Fig.10 presents TSA results under a dynamic transition from 0.95 leading PF to UPF at t = 5 s, coupled with a step adjustment in the reference peak injected grid current from 10 A to 12.295 A. Subfigure (a) illustrates the input DC source voltage profile, which remains stable at Vdc = 100 V during the transient. Subfigure (b) demonstrates balanced DC-link CVs, consistently regulated at 200 V despite the operational shift. Subfigure (c) showcases the five-level IOV, maintaining its peak magnitude of ±400 V throughout the transition.

Subfigure (d) captures the system's response to the leading PF-to-UPF shift, highlighting the PR-control strategy's ability to simultaneously govern leading RPC and APC with precision. These outcomes validate the controller's adaptability in managing capacitive-to-resistive load transitions, ensuring robust voltage regulation, harmonic attenuation, and seamless power factor correction under transient conditions.

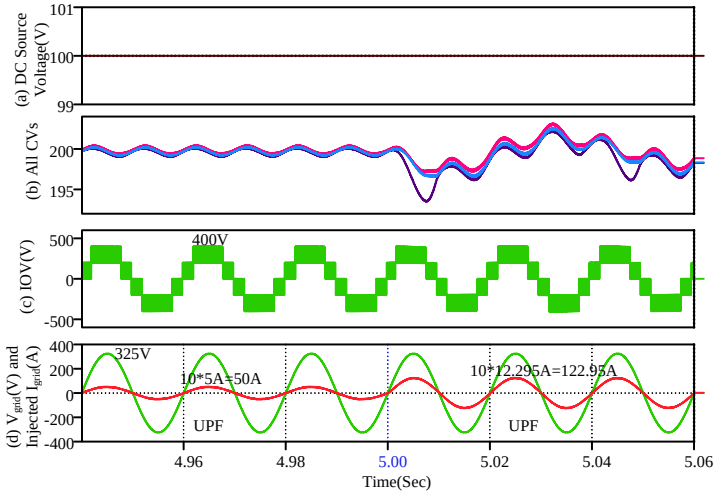


Fig.11 TSA results (UPF: reference peak grid current =5A to 12.295A at t=5sec): GTI Operation

Fig.11 demonstrates TSA results under a dynamic step change in the reference peak injected grid current from 5 A to 12.295 A at t = 5 s during UPF operation. Subfigure (a) illustrates the input DC source voltage profile, regulated to a stable Vdc = 100 V throughout the transient. Subfigure (b) confirms balanced DC-link CVs, maintained at 200 V despite the abrupt current adjustment.

Subfigure (c) depicts the five-level IOV waveform, sustaining its peak amplitude of ±400 V during the transition. Subfigure (d) captures the system's UPF operation, validating the PR-control strategy's efficacy in achieving precise APC with minimal oscillation during the step change. These results emphasize the controller's robustness in managing rapid current reference variations, ensuring voltage stability, harmonic suppression, and seamless power delivery under dynamic grid conditions.

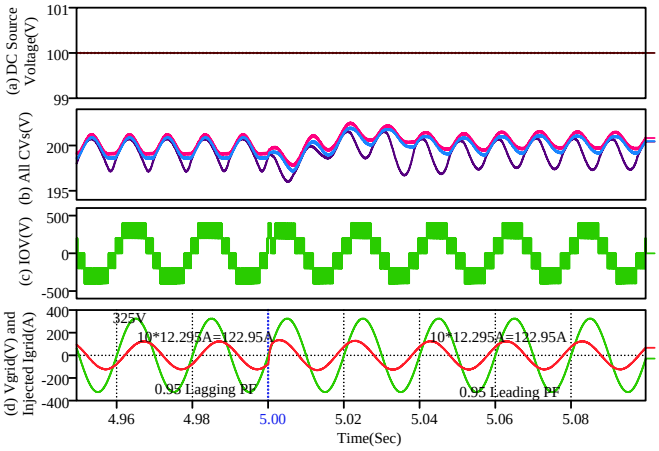


Fig.12 TSA results (0.95 lagging PF to 0.95 leading PF at t=5sec): GTI Operation

Fig. 12 presents TSA results under a dynamic transition from 0.95 lagging to 0.95 leading PF at t = 5 s, with a fixed reference peak injected grid current of 12.295 A. Subfigure (a) illustrates the input DC source voltage profile, which remains stable at Vdc = 100 V during the transient. Subfigure (b) demonstrates balanced DC-link CVs, consistently regulated at 200 V despite the bidirectional reactive power shift. Subfigure (c) depicts the five-level IOV, maintaining its peak amplitude of ±400 V throughout the transition.

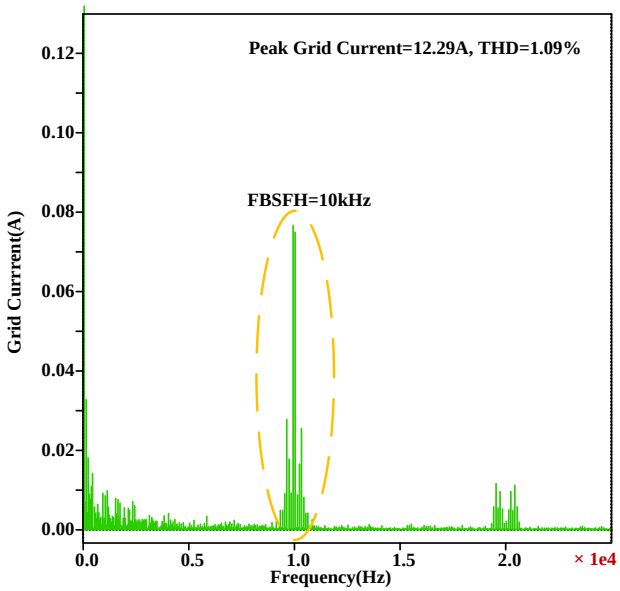


Fig.13 Harmonic Spectrum of Grid Current-UPF Operation

Fig. 13 illustrates the harmonic spectrum analysis of the injected grid current during UPF operation, achieving a total harmonic distortion (THD) of 1.09%, which aligns with the rigorous IEEE-519 harmonic compliance standards. This result underscores the system's exceptional harmonic suppression capabilities, ensuring minimal distortion and high-fidelity sinusoidal current injection into the grid—a critical requirement for maintaining power quality and operational reliability in modern grid-connected renewable energy systems.

In conclusion, the comprehensive analysis of above all case studies validates that the PR control strategy, integrated with the proposed M5L-NPC GTI topology and FE-MLBC, demonstrates exceptional dynamic performance and steady-state accuracy. The system achieves precise current reference tracking, robust APC, and RPC under diverse operating scenarios, including power factor transitions, step changes in current references, and bidirectional reactive load variations. These results highlight the topology's ability to maintain voltage balance, suppress harmonics, and ensure seamless power quality compliance, even during transient disturbances, thereby affirming its suitability for high-performance renewable energy integration and modern grid applications requiring

adaptive power flow management.

III. CONCLUSION

In conclusion, this study introduces a novel M5L-NPC inverter topology, designed to overcome the inherent limitations of conventional 5L-NPC architectures. While traditional 5L-NPC systems, powered by dual rigid DC sources and governed by LS-PWM, suffer from elevated conduction losses due to bidirectional switches reliant on diode-IGBT combinations and persistent challenges in DCL-CV balancing, the proposed M5L-NPC configuration integrates a FE-MLBC. This innovative approach autonomously regulates DCL-CV imbalances while achieving voltage amplification at reduced duty cycles, eliminating dependency on external voltage sensors and complex control algorithms.

The topology's efficacy is demonstrated across both standalone and grid-connected operational modes, with the latter emphasizing critical grid synchronization objectives, including RPC, APC, and low-distortion sinusoidal current injection. A simplified PR control strategy is shown to effectively harmonize these objectives, ensuring compliance with power quality standards. By mitigating switching losses, enhancing voltage regulation, and streamlining control complexity, the M5L-NPC topology advances the feasibility of robust, efficient multilevel inverters for modern renewable energy systems and smart grid applications.

REFERENCES

[1] Singh, V. Jately, P. Kala, Y. Yang and B. Azzopardi, "Advancements in Multilevel Inverters for Efficient Harnessing of Renewable Energy: A Comprehensive Review and Application Analysis," in IEEE Access, vol. 12, pp. 156939-156964, 2024, doi: 10.1109/ACCESS.2024.3477501.

[2] S. Munawar, M. S. Iqbal, M. Adnan, M. Ali Akbar and A. Bermak, "Multilevel Inverters Design, Topologies, and Applications: Research Issues, Current, and Future Directions," in IEEE Access, vol. 12, pp. 149320-149350, 2024, doi: 10.1109/ACCESS.2024.3472752.

[3] R. F. Yehia, R. B. Gonzatti, Z. Guo, H. Li and F. Z. Peng, "Low Frequency Versus High Frequency PWM in Medium Voltage, High Power, Higher Level Inverters: THD, Harmonic Filtering, and Efficiency Comparison," in IEEE Open Journal of Power Electronics, vol. 5, pp. 1404-1418, 2024, doi: 10.1109/OJPEL.2024.3458891.

[4] S. S. Lee, "Switched-Midpoint Boost Inverter (SMBI)," in IEEE Transactions on Industry Applications, vol. 61, no. 1, pp. 463-471, Jan.-Feb. 2025, doi: 10.1109/TIA.2024.3476449.

[5] S. P. D. Kumar, B. K. Murthy and A. Bhanuchandar, "Implementation of Predictive Current Control Technique for a 1-Phase 5-Level Switched Capacitor-Based Grid-Connected Inverter," 2024 International Conference on Intelligent Algorithms for Computational Intelligence Systems (IACIS), Hassan, India, 2024, pp. 1-6, doi: 10.1109/IACIS61494.2024.10721969.

[6] K. Palle, S. Vattikonda, S. S. Vangala, K. Tammali, A. Bhanuchandar and A. Mohandas, "A Generalized Non-Carrier Modulation Technique for an Asymmetric Source Configuration of Single-Phase CHB-MLI Topology Using PLECS Tool," 2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT), Hyderabad, India, 2022, pp. 1-5, doi: 10.1109/SeFeT55524.2022.9909071.

[7] K. Tammali, S. S. Vangala, S. Vattikonda, K. Palle, A. Bhanuchandar and K. B. Kumar, "An Asymmetric Source Configuration of Single-Phase CHB-MLI Topology with a Generalized Reduced-Carrier Modulation Technique," 2022 International Conference on Intelligent Controller and Computing for Smart Power (ICICCSP), Hyderabad, India, 2022, pp. 1-5, doi: 10.1109/ICICCSP53532.2022.9862515.

[8] K. B. Kumar, A. Bhanuchandar, B. Supriya, D. Vamshy, K. Palle and R. Sakile, "A Unipolar Phase Disposition Pulse Width Modulation Technique for an Asymmetrical Multilevel Inverter Topology," 2021 IEEE International Conference on Intelligent Systems, Smart and Green Technologies (ICISSGT), Visakhapatnam, India, 2021, pp. 156-161, doi: 10.1109/ICISSGT52025.2021.00041.

[9] Bhanuchandar and B. K. Murthy, "Switched Capacitor Based 13-Level Boosting Grid Connected Inverter with LCL Filter," 2021 National Power Electronics Conference (NPEC), Bhubaneswar, India, 2021, pp. 01-06, doi: 10.1109/NPEC52100.2021.9672544.

[10] R. Sakile, A. Bhanuchandar, K. B. Kumar, D. Vamshy, B. Supriya and K. Palle, "A Nearest Level Control Scheme for Reduced Switch Count Cascaded Half-Bridge Based Multilevel DC Link Inverter

Topology," 2021 8th International Conference on Signal Processing and Integrated Networks (SPIN), Noida, India, 2021, pp. 287-292, doi: 10.1109/SPIN52536.2021.9566056.

[11]Bhanuchandar and B. K. Murthy, "Single Phase Nine Level Switched Capacitor Based Grid Connected Inverter with LCL Filter," 2020 3rd International Conference on Energy, Power and Environment: Towards Clean Energy Technologies, Shillong, Meghalaya, India, 2021, pp. 1-5, doi: 10.1109/ICEPE50861.2021.9404491.

[12] K. B. Kumar, A. Bhanuchandar and C. Mahesh, "A Novel Control Scheme for Symmetric Seven Level Reduced Device Count Multi-Level DC Link (MLDCL) Inverter," 2021 International Conference on Sustainable Energy and Future Electric Transportation (SEFET), Hyderabad, India, 2021, pp. 1-4, doi: 10.1109/SeFet48154.2021.9375714.

[13] Tiwari, V. Kumar, R. Agarwal, M. Amir, M. A. Alharbi and S. M. Muyeen, "Five-Level MLI-Based Grid-Connected Photovoltaic Systems: A Review on Control Methodologies, Modulation Strategies and Recent Developments," in IEEE Open Journal of Power Electronics, vol. 6, pp. 78-108, 2025, doi: 10.1109/OJPEL.2024.3515288.

[14] M. R. A and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," in IEEE Transactions on Industrial Electronics, vol. 62, no. 12, pp. 7569-7577, Dec. 2015, doi: 10.1109/TIE.2015.2455523.

[15] R. Goel, D. Etta, R. V. Chavali and A. Dey, "A Fault Tolerant Modulation Scheme for a Hybrid Multilevel Inverter in the Event of Open-Switch Fault," in IEEE Transactions on Power Electronics, vol. 40, no. 3, pp. 3861-3872, March 2025, doi: 10.1109/TPEL.2024.3486006.

[16] H. Wang, J. Zhang, X. Xia, F. Gao and J. Cheng, "DC-Link Capacitance Design for Cascaded H-Bridge STATCOM With Sum of Squares Formulation," in IEEE Transactions on Power Electronics, vol. 39, no. 5, pp. 5733-5749, May 2024, doi: 10.1109/TPEL.2024.3365178.

[17]S. Srikanthan and M. K. Mishra, "DC Capacitor Voltage Equalization in Neutral Clamped Inverters for DSTATCOM Application," in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2768-2775, Aug. 2010, doi: 10.1109/TIE.2009.2022069.

[18] Kumar, Y. & Tangirala, Murali & Guduri, Yesuratnam. (2024). Single-phase five level modified neutral point clamped grid connected inverter topology with front-end chopper control of DC-link capacitor voltages. International Journal of Power Electronics and Drive Systems (IJPEDS). 15. 2287. 10.11591/ijpeds.v15.i4.pp2287-2295.

[19] A. Choubey, P. K. Padhy and S. K. Jain, "Model Predictive control for DC-DC Boost converter," 2021 IEEE Conference on Energy Conversion (CENCON), Johor Bahru, Malaysia, 2021, pp. 58-63, doi: 10.1109/CENCON51869.2021.9627268.

[20] Y. Li, S. Sahoo, T. Dragičević, Y. Zhang and F. Blaabjerg, "Stability-Oriented Design of Model Predictive Control for DC/DC Boost Converter," in IEEE Transactions on Industrial Electronics, vol. 71, no. 1, pp. 922-932, Jan. 2024, doi: 10.1109/TIE.2023.3247785.

[21] J. C. Rosas-Caro, J. M. Ramirez and P. M. Garcia-Vite, "Novel DC-DC Multilevel Boost Converter," 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 2008, pp. 2146-2151, doi: 10.1109/PESC.2008.4592260.

[22] Mayo-Maldonado, Jonathan & Salas-Cabrera, R. & Caro, Julio & De León-Morales, Jesus & Salas-Cabrera, E.N.. (2011). Modelling and control of a DC-DC multilevel boost converter. IET Power Electronics. 4. 693 - 700. 10.1049/iet-pel.2010.0191.

[23] S. Habibi, R. Rahimi, M. Ferdowsi and P. Shamsi, "A General Method for Analyzing Single-Switch Step- Up DC–DC Converters With Switched-Capacitor Cells and an Output Inductor," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 5, no. 3, pp. 858-867, July 2024, doi: 10.1109/JESTIE.2023.3328809.

[24] Priyadarshi, P. K. Kar and S. B. Karanki, "A Single Source Transformer-Less Boost Multilevel Inverter Topology With Self-Voltage Balancing," in IEEE Transactions on Industry Applications, vol. 56, no. 4, pp. 3954-3965, July-Aug. 2020, doi: 10.1109/TIA.2020.2988012.

BIOGRAPHIES OF AUTHORS

	**Y Sravan Kumar**, is a research scholar at department of Electrical Engineering, Osmania university. He has obtained his Masters and Bachelor from Jawaharlal Nehru Technological University, Hyderabad, India in 2011 and 2008 respectively. He worked as an Associate professor and Assistant professor for over a decade. His research interests include Control Systems, Power Electronics, and Electromagnetic fields. **ORCID : https://orcid.org/0009-0004-7017-3713**
	**T Murali Krishna** received UG degree from the Institution of Engineers (India), Kolkata in 2001, M. Tech in Electrical Power Systems, and PhD from JNTUA, Anantapuramu, Andhra Pradesh in 2005 and 2016, respectively. He is presently working at Chaitanya Bharathi Institute of Technology as an Associate Professor in the Department of EEE. His research interests include Power Electronics, FACTS, Wavelets, Renewable Energy Integration etc. **ORCID : https://orcid.org/0000-0001-9597-1229**
	**Yesuratnam Guduri**, received B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India in 1995. He received M.Tech. degree in 1998 from Regional Engineering College, Warangal in the field of power systems. He received Ph.D. degree from the Department of Electrical Engineering, Indian Institute of Science, Bangalore in 2007. Currently he is working as Senior professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad. His research interests include computer aided power system analysis, reactive power optimization, Voltage stability and artificial intelligence applications in power systems.