Journal of Information Systems Engineering and Management
2025, 10(24s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

Review on the Design of Meminductor Emulator Using Analog Building Blocks

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ARTICLE INFO

Received: 18 Dec 2024
Revised: 05 Feb 2025
Accepted: 18 Feb 2025

ABSTRACT

The advent of meminductors as a basic passive circuit element has sparked widespread attention because of their potential uses in neuromorphic computing, memory storage, and programmable analog circuits. This study gives a detailed assessment of design techniques for meminductor emulators, emphasizing current-mode components. Current-mode circuits provide benefits such as fast operation, low power consumption, and a greater dynamic range, making them an excellent option for meminductor emulator design. The study categorizes and analyzes current designs based on their fundamental ideas, circuit design, and performance metrics. The challenges of precise emulation, robustness, and compatibility with contemporary integrated circuit technology are explored. The study also focuses on emerging trends, prospective applications, and prospects for research in this discipline. This study seeks to serve as a helpful resource for academics and practitioners, offering insights on state-of-the-art developments and influencing the growth of creative microcontroller emulation approaches.

Keywords: Meminductor, Emulator, Current mode building block (CMBB).

INTRODUCTION

The fundamental circuit elements-resistor (R), capacitor (C), and inductor (L) are identified by particular relationships: The resistance, which quantifies the rate at which voltage changes about current, the inductance, which quantifies the rate at which flux changes about current, and the capacitance, which characterizes the rate at which charge changes about voltage However, the missing relationship between flux and charge [1]. Leon O. Chua proposed the memristor, a fourth element, in 1971 to solve the problem of the lack of correlation between charge and the rate of flux change [2]. Not long after that, 38 years later, he reveals its twins, the memcapacitor and the meminductor [3]. Combining all these three is called memory elements. They have memory dependent behavior; they can store their last state of input variable, so output is dependent on the history of input variable [4]. Even the power is removed Their memory is retained. Memelement exhibits a wide frequency response, meaning they are capable of operating across a broad range of signal frequencies [5]. This makes them suitable for high-speed applications, such as in communication systems or dynamic circuits, where fast switching and responsiveness are crucial [6]. Meminductors, an interesting family of memory-enabled inductive components, have lately gained interest in the electronics industry due to their unusual capability to preserve memories of previous states [7]. These elements behave dynamically with magnetic flux and charge in the same manner as memristors and memcapacitors do they have also shown promise in programmable analog circuits, programmable electronics, and non-volatile memory storage systems, where their storage capacity may boost effectiveness & adaptability [8]. Despite their theoretical promise, meminductors have been difficult to deploy in practice. Physical meminductors are difficult to fabricate because of material constraints and the challenge of getting the required characteristics [9]. These constraints have prompted the creation of meminductor emulators, which are circuit implementations that replicate the activities of meminductors without needing actual construction [10]. Emulators provide a realistic approach to investigate meminductor technology and incorporate them into current electrical systems [11].

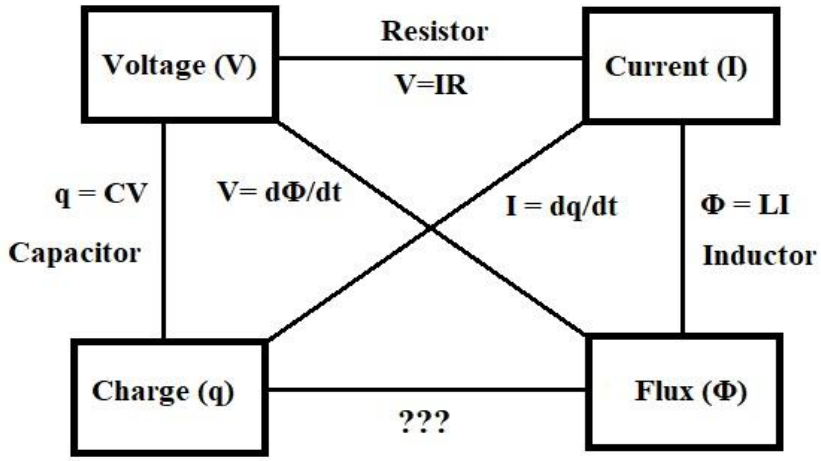


Figure 1. Missing relation between elements

A meminductor is an extension of the memristor notion that is used in passive circuits in theory [12]. The meminductor combines inductive behaviour with memory device characteristics. In the same way that a resistor links voltage (V) and current (I) by referring Fig. 1, it forms a connection between charge (q) and magnetic flux (ϕ) (the time integral of voltage).

For resistor,

$$\boldsymbol{V = I * R} \tag{1}$$

For Inductor,

$$\boldsymbol{\phi = L * I} \tag{2}$$

For Capacitor,

$$\boldsymbol{q = C * V} \tag{3}$$

Where Φ is the magnetic flux and L is the self-inductance. For a memristor, multiplying with (dt) on both sides and integrating,

$$\boldsymbol{\int V\, dt \;=\; \int I * R\, dt} \tag{4}$$

$$\boldsymbol{\int \frac{d\phi}{dt}\, dt = R \int I\; dt} \tag{5}$$

The integral of current is Charge(q), so

$$\boldsymbol{R \int I\, dt = q * R} \tag{6}$$

$$\boldsymbol{\phi = q * R} \tag{7}$$

$$\boldsymbol{V \;=\; \frac{d\Phi}{dt} \;=\; \frac{d\Phi}{dq}\; x\; \frac{dq}{dt} \;=\; R(q) \cdot\; i(t)} \tag{8}$$

$$\boldsymbol{\frac{d\Phi}{dt} \;=\; R(q)} \tag{9}$$

$R(q)$or M_R is called the memristance.

$$\mathbf{i}(\boldsymbol{t}) = \frac{\boldsymbol{dq}}{\boldsymbol{dt}} = \frac{\boldsymbol{dq}}{\boldsymbol{d\Phi}} \boldsymbol{x} \frac{\boldsymbol{d\Phi}}{\boldsymbol{dt}} = \boldsymbol{G}(\boldsymbol{\Phi}) \cdot \boldsymbol{v}(\boldsymbol{t}) \quad (10)$$

$$\boldsymbol{G}(\boldsymbol{\Phi}) = \frac{\boldsymbol{dq}}{\boldsymbol{d\Phi}} \quad (11)$$

$G(\Phi)$ *or* ML is called the mem inductance.

Despite its theoretical foundation, the meminductor has not yet been implemented physically. Some researchers are working on an emulation circuit of meminductors and using them in different applications [13].

Among the several methods of microprocessor emulation, current-mode components have become a reliable and efficient choice [14]. Unlike voltage-mode circuits, current-mode circuits handle signals as currents. This yields quicker reaction times, lower power consumption, and a wider dynamic range, making them ideal for high-speed, low-power applications [15]. Furthermore, current-mode building blocks are well-suited to contemporary semiconductor technologies, resulting in scalability and compatibility with integrated circuit designs. Because of these advantages, current-mode circuits are often used to build meminductor emulators [16].

Several designs for meminductor emulators have been suggested, each using a unique current-mode building component, such as current conveyors, current differencing transconductance amplifiers (CDTAs), and operational transconductance amplifiers [17]. These designs strive to accurately emulate the flux-charge properties of meminductors while being small, and energy efficient. Certain designs encourage linearity in the emulator's behavior, whilst others prioritize flexibility to application needs, such as neuromorphic computing or programmable analog filters. However, difficulties like as non-idealities, parasitic effects, and circuit complexity persist, demanding more research in this area [18].

The major goal of this study is to offer a comprehensive overview of the design and implementation of meminductor emulators utilizing current mode building blocks [19]. The purpose of this study is to identify the strengths and limits of current systems, examine their performance indicators, and offer prospective areas for growth based on cutting-edge innovations. The focus is on exploring circuit layouts, design concepts, and emulation practicality [20].

This research also attempts to investigate the broader implications of microprocessor emulators for current and future technology [21]. The study intends to spark new ideas and help researchers construct future semiconductor emulators by investigating the integration possibilities with complex systems as well as the limitations of scaling such designs for commercial use [22]. Furthermore, recent breakthroughs in current-mode circuit design and their application to meminductor emulation are discussed, offering insight into the field's future potential [23]. Meminductors are especially well-suited for new applications such as neuromorphic computing, where their ability to recreate synaptic activity has the potential to alter artificial neural network design [24].

Finally, this paper provides a full overview of the design and implementation of microprocessor emulators, with an emphasis on current-mode components [25]. It aims to eliminate the disconnect between theoretical breakthroughs and actual implementations, enabling semiconductor emulators to be employed in a variety of applications [26]. By doing so [27], it wants to contribute to the advancement of electronics and open the door to creative applications that utilize the unique qualities of meminductors [28].

LTERATURE REVIEW

2.1 Circuit elements with memory: Memristors, memcapacitors, and meminductors, Massimiliano Di Ventra, et.al. (2009) [2]

Study conducted the concept of memristive systems to include elements with capacitive as well as inductive characteristics, including inductors and capacitors, whose characteristics are dependent on the system's current and past states. The two constitutive variables that determine each of these elements—current-voltage for the memristor, charge-voltage for the memcapacitor, and current-flux for the meminductor—show constricted hysteretic loops. The dynamical characteristics of electrons and ions are anticipated to be system-dependent, at least within specific time scales, at the nanoscale, where such devices are prevalent, according to our argument. Neuromorphic systems that mimic learning, flexible, and impulsive actions are expected to make use of these components and their circuit

combinations, which open up new functions in electronics. In this study, as per definition Nth order current controlled meminductor described as,

$$\boldsymbol{\varphi(t) = L\,(x, I, t) I(t)} \tag{12}$$

Final equation of current controlled meminductor is,

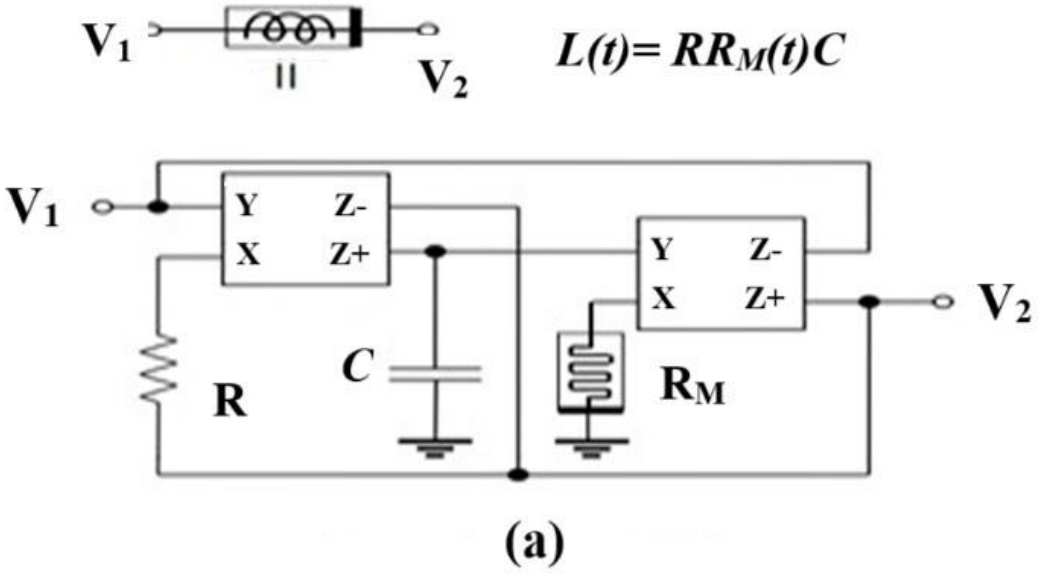
$$\boldsymbol{\varphi(t) = L\left[\int_{to}^{t} I\,(\tau)\ d\tau\right] I(t)} \tag{13}$$

Where φ(t) is the flux (or magnetic flux) at time t. L is the meminductance. I(t) is the current at time t. $\int_{to}^{t} \boldsymbol{I\,(\tau)\ d\tau}$ represents the total charge accumulated from time to to t, which is essentially the charge that has flowed through the system.

2.2 Emulation of floating memcapacitors and meminductors using current conveyors, Yuriy V. Pershin, et.al. (2011) [3]

Research performed to make memristive devices work as memcapacitive and meminductive systems on the fly, Reserchers propose circuit realizations of emulators which is shown in Fig. 2. The emulator's circuits utilize either two dual-output or four single-output current conveyors based on second-generation technology. We give the equations that control the memcapactive and meminductive systems that emerge from this. In this paper the following equations are governing meminductance behaviour, φ is the flux, L is the meminductance.

$$\boldsymbol{I = \frac{1}{CRRM\left(x, \frac{\varphi}{RC}, t\right)} \varphi \equiv [L(x, \varphi, t)]^{-1}\, \varphi} \tag{14}$$



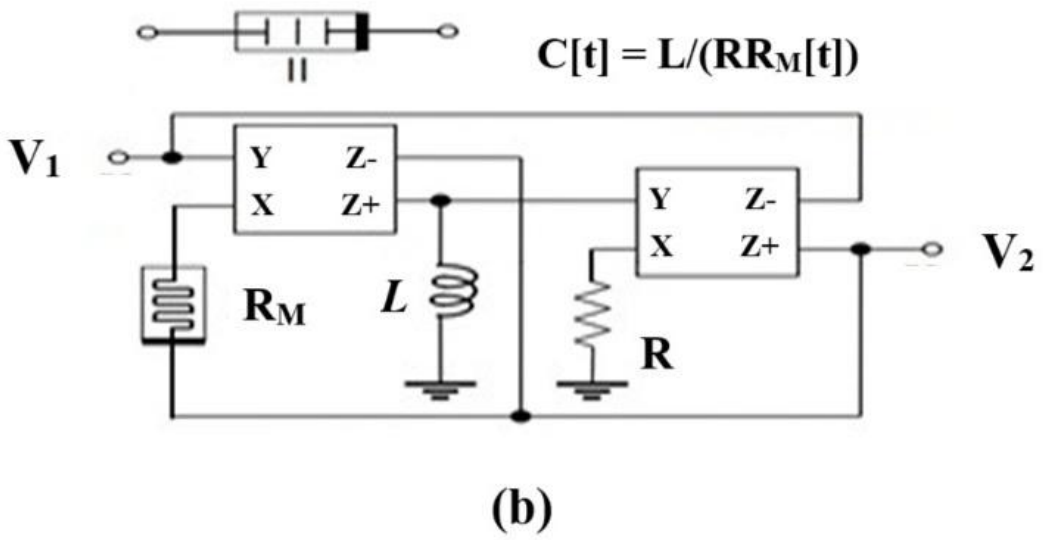


Figure 2. (a) Emulators of meminductive (b) memcapacitive systems employing dual-output current conveyors

2.3 Research performed to make memristive devices work as Chaos in a Meminductor-Based Circuit Fang Yuan, et.al. (2016) [5]

Research was carried out using the premise that meminductors are often inaccessible, and an example of a meminductor's smooth curve and the associated circuit was developed. You may use a similar circuit to try out various layouts for meminductor application circuits on a breadboard. This paper presents a chaotic oscillator that is based on meminductor technology. The dynamical map of the system, bifurcations, the equilibrium set, and the spectrum of Lyapunov exponents are among the dynamical properties of the oscillator studied. The focus here is on amplitude control, and we find coexisting attractor instances with different parameter values. The findings from the experiments of the meminductor-based oscillator and the meminductor model are also presented to show how they were corrected.

In this paper, the inverse meminductance is assumed as

$$L^{-1} = a + b\rho^2 \tag{15}$$

Then the nonlinear current-flux relationship of the meminductor can be defined as follows,

$$I(t) = \left(a + b\rho^2\varphi(t)\right) \tag{16}$$

$$\rho^{\cdot} = \varphi(t) \tag{17}$$

To obtain a flux-controlled meminductor as described by (15), an equivalent circuit consisting of four operational amplifiers U1, U2, U3, U4 and two multipliers was designed, as shown in this circuit implementation in Fig. 3, it is assumed that all the components are ideal without losses.

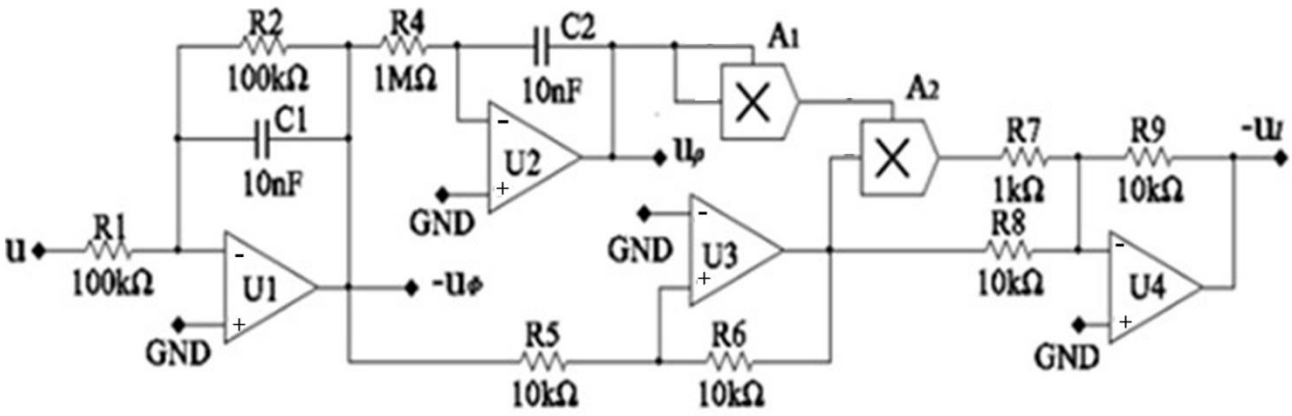


Figure 3. The equivalent circuit of the flux-controlled meminductor

2.4 A simple floating mutator for emulating memristor, memcapacitor, and meminductor, Dongsheng Yu, et.al. (2020) [6]

Research performed using a varactor diode with a variable capacitance, this short presents a newly built, simple floating mutator circuit that can change between memristor (MR), memcapacitor (MC), and meminductor (MI) emulations. In this paper, a circuit given in Fig. 4, there are 1 and 2, which are assign for components resistor or capacitor or varactor diode as per required emulator circuit. For meminductor emulator circuit components are in frame is varactor diode and resistor, and its final equation of meminductor emulator is derived in this paper,

$$\boldsymbol{L(q)} = \frac{\boldsymbol{R1\,R2\,C2}}{\boldsymbol{\alpha C1}} \left(\boldsymbol{\alpha_0 + \alpha_1 v_1 + \alpha_2 {v_1}^2}\right) \tag{18}$$

where,

$$\boldsymbol{v_1} = \frac{\boldsymbol{q_{AB}}}{\boldsymbol{C_1}} \quad , \quad \boldsymbol{V_{DC} = 0\ V} \tag{19}$$

The passive components in the two preserved locations of the mutator circuit need to be configured correctly to accomplish the transformation. The floating terminals, which do not need any mem-elements for transformation, are the most appealing feature of this mutator. For integrated circuit design, the mutator topology is ideal since it is straightforward. The novel mutator's feasibility and adaptability are confirmed by the reported experimental & simulation findings.

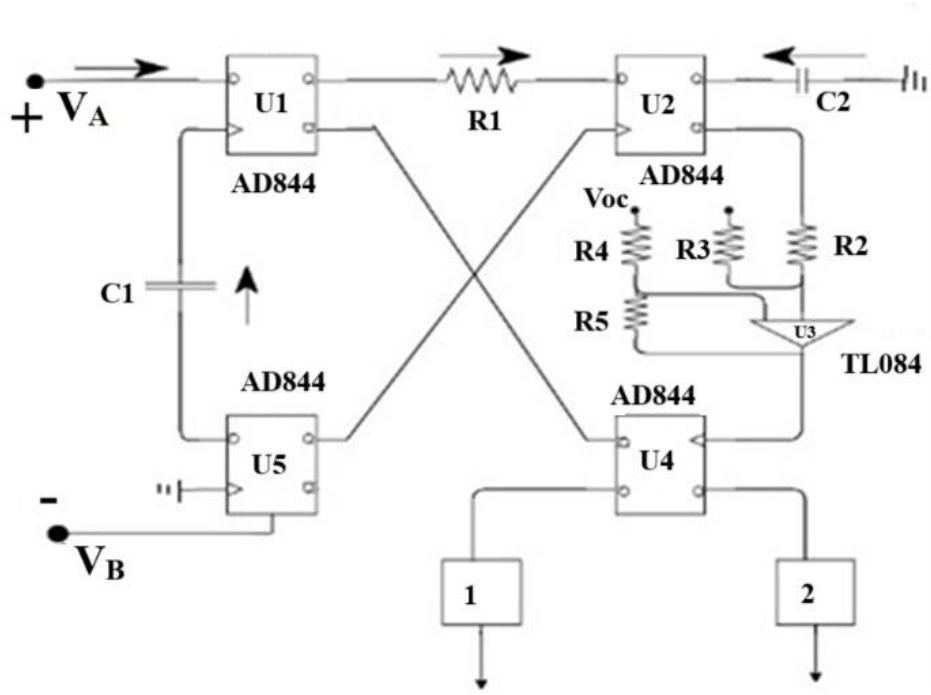


Figure 4. Mutator circuit

2.5 A Novel Floating/Grounded Meminductor Emulator, Hasan Sozen, et.al. (2020) [7]

Research performed having the capacity to store energy and remember past events, meminductors are nonlinear two-terminal elements. There is currently not a readily accessible meminductor element, however there are memristor and memcapacitor alternatives. Consequently, a meminductor emulator for breadboard experiments is quite important. Without the use of a memristor, this article presents a flux-controlled floating/grounded meminductor emulator. Emulator circuit shown in Fig. 5, It has one operational amplifier, one multiplier, two current conveyors of the second generation (CCIIs), one current feedback operational amplifier (CFOA), and one operational transconductance amplifier (OTA). The size of the pinched hysteresis loop of the meminductor may be controlled using an extra parameter introduced by the OTA device, in addition to the amplitude and frequency values of the applied voltage. To illustrate the operation of the meminductor circuit, a mathematical model of the suggested emulator circuit is provided. For the breadboard experiment, they used the following components: CA3080 for the operational amplifier, AD844, AD633J for the multiplier, and LM741 for the CCII-CFOA. Validation of the theoretical studies is provided by means of experimental and simulation test findings. The constricted hysteresis loop, which is frequency dependent, is maintained up to 5 kHz. At higher frequencies, the meminductor emulator acts more like a regular inductor. In this paper researcher has given inverse flux control meminductance equation suggests a relationship between the inverse meminductance (L_m^{-1}) and various circuit parameters, including the transconductance (g_m), resistances (R_5, R_6, R_2, R_4), capacitances (C_1, C_2), resistivity (ρ), and a voltage (v_5).

$$L_m^{-1} = \frac{g_m^2 R_5}{10 C_1^2 C_2 R_2 R_6}\,\rho + \frac{g_m^2 R_5}{10 C_1 R_4 R_6} v_5 \qquad (20)$$

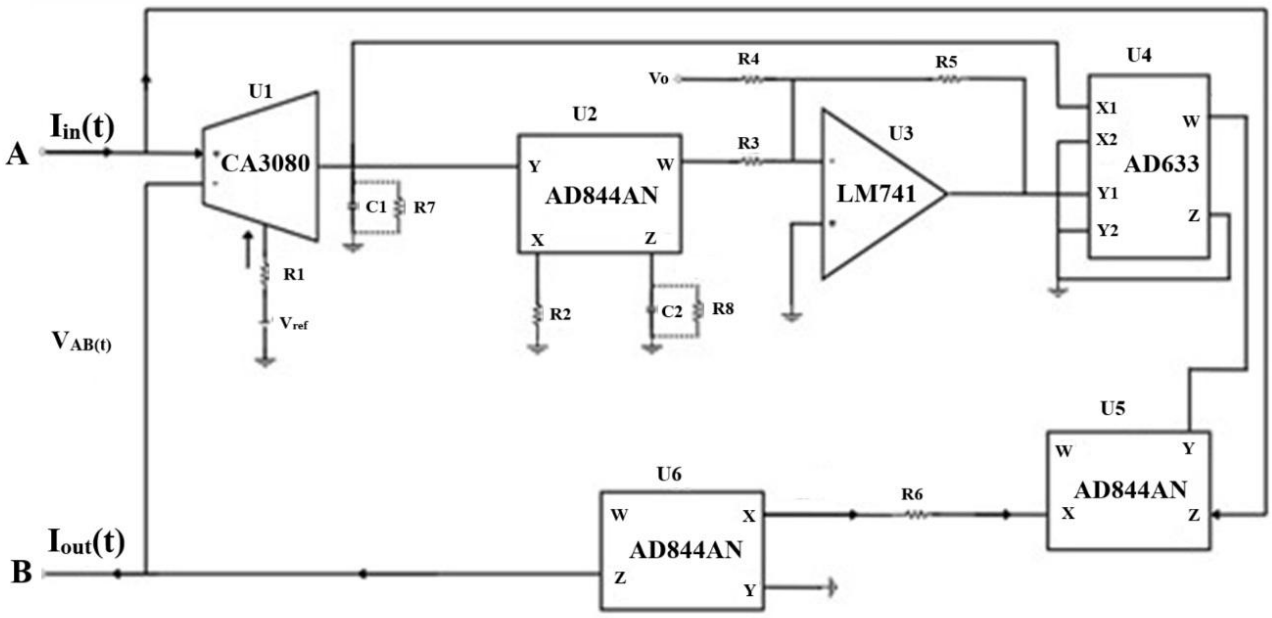


Figure 5. Emulator circuit for meminductor

2.6 High Frequency Meminductor Emulator Employing VDTA and its Application, John Vista, et.al. (2020) [8]

Study conducted incorporating a voltage difference transconductance amplifier (VDTA), this study presents a grounded and floating meminductor. Each of the suggested meminductor models has a total of two grounded capacitors & two active VDTAs shown in Fig. 6. Using post-layout simulation in the Cadence Virtuoso tool and experimentally utilizing off-the-shelf components like operational transconductance amplifiers (OTAs) for VDTA implementation with passive components, the performance assessment of the suggested meminductor is confirmed. Literature also extensively covers the execution of neuromorphic circuits as an application of the suggested meminductor. The equivalent inverse meminductance is given as, $\boldsymbol{Lm^{-1}}$represents the inverse of an meminductance, which suggests the equation is related to an inductive element in the circuit., gm1 and gm2These are the transconductance values of two VDTA. The transconductance indicates how efficiently the input voltage is converted into output current.C1 and C2 These are capacitors, likely involved in determining the frequency response or the behavior of the circuit. ρ(t) This represents a time-varying resistivity.

$$\boldsymbol{L_M^{-1} = \frac{g_{m_1} g_{m_2}}{C_1}\left[1 \neq \frac{g_{m_1} g_{m_2}}{10 C_1 C_2}\rho(t)\right]} \quad (21)$$

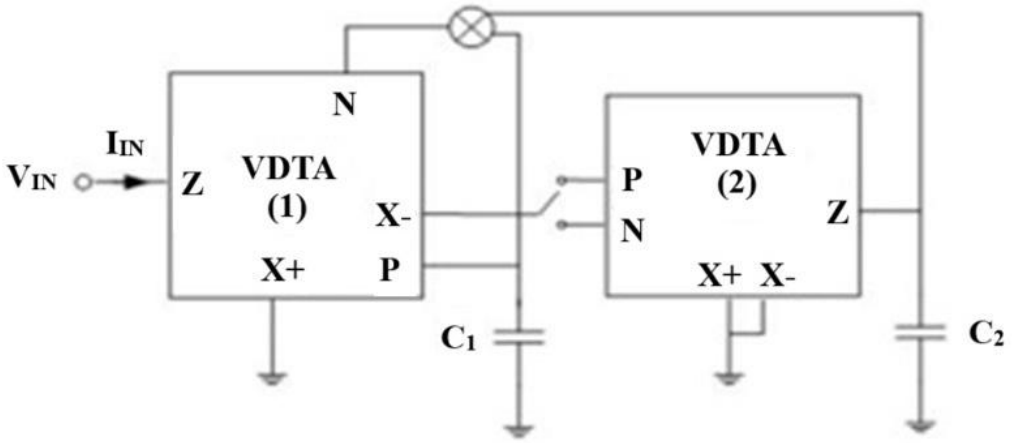


Figure 6. Configuration for (a) decremental mode (b) incremental mode

2.7 Novel Floating and Grounded Memory Interface Circuits for Constructing Mem-Elements and Their Applications. Yue Liu, et.al. (2020) [9]

Study conducted the memristor, memcapacitor, and meminductor are all examples of memory components. They are seen as essential for creating the next wave of neuromorphic and intelligent technology. My research and commercialization efforts in mem-element devices are hindered by their difficulty to build, which is a result of the complex nano-scale manufacturing technology. Another way to enhance knowledge in mem-elements research is the upcoming independent/universal emulators. To ensure that circuit theory is comprehensive, this paper explains three mem-elements and their mathematical representations, categorizes them, and introduces the idea of unfolding with an expanded formulation. Next, the mathematical model, fingerprints, and newly suggested floating/grounded memory interface circuits with a broad frequency range are introduced. Furthermore, we highlight the primary frequency-influencing elements and prove that memristors can reach frequencies of up to 900 kHz and memcapacitors can reach frequencies higher than 500 kHz. We conclude by investigating a possible use case for the interface circuit—a basic chaotic circuit—that has been suggested. Additionally, three chaotic systems including a mem-element have their models, peculiar attractor terms, and Lyapunov exponents calculated, accordingly. The reliability and adaptability of these interface circuits have been confirmed by the high degree of agreement between theoretical analysis, simulation, and experimental outcomes. The grounded MC emulator circuit and symbol is shown in Fig. 7.

The equivalent inverse meminductance is given as, where, iLM is the current through the meminductor. φM is the magnetic flux associated with the meminductor. gLM is the transconductance, defined as the ratio of current to flux. ρM is the resistivity associated with meminductance.

$$g_{L_M} = \frac{i_{L_M}}{\varphi_M} = \frac{R_4}{10RxR_1^2R_3R_5C_1^2C_2}\rho_M + \frac{R_4}{R_xR_1R_2C_1} \tag{22}$$

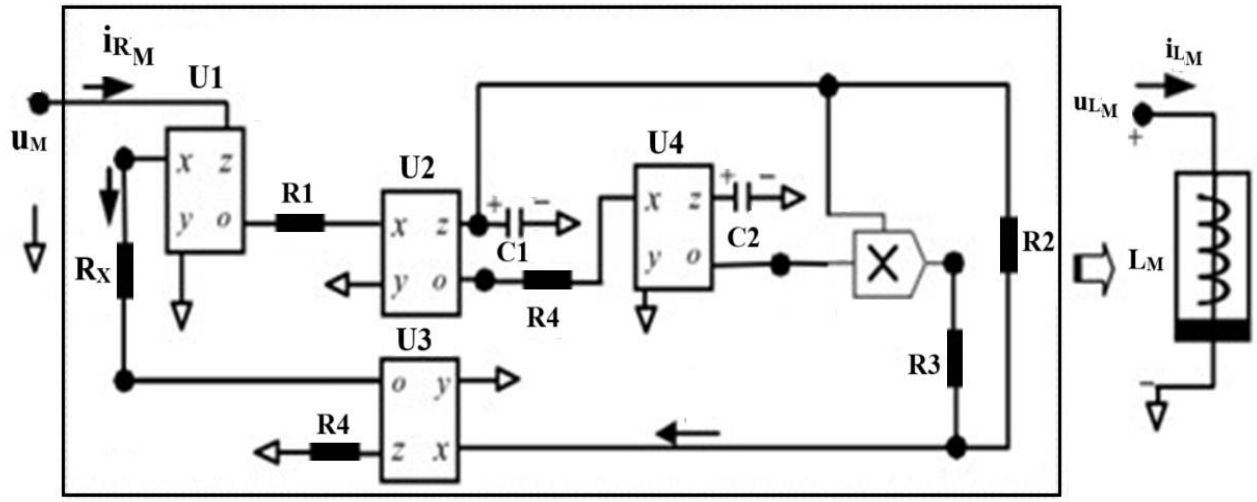


Figure 7. The grounded MC emulator circuit and symbol

2.8 High -Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and its application as AM Modulator, Pratik Kumar, et.al. (2023) [23]

A study conducted a new design has been for the realization of grounded and floating meminductor emulators built with two OTAs and two second-generation current conveyors shown in Fig. 8 and Fig. 9. The emulators can be configured in both incremental and decremental topology. This paper also proposes the application of meminductor as Amplitude Modulator (AM). The circuits and its application claim that the circuit is much simpler in design and can be utilized in both topologies. The performance of all the circuits has been verified with Cadence Virtuoso Spectre using standard CMOS 180nm. Furthermore, post-layout simulations and its comparison along with non-ideal and Monte Carlo analysis have been carried out in detail.

$$L_M^{-1} = \frac{\phi_{in}}{I_{in}} \approx \frac{k}{\sqrt{2}R_1C_2}(Vss + 2Vth)\frac{\pm k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_1^2C_2^2}\right) \quad (23)$$

where for the operator ±, the + is for incremental and – is for decremental configuration.

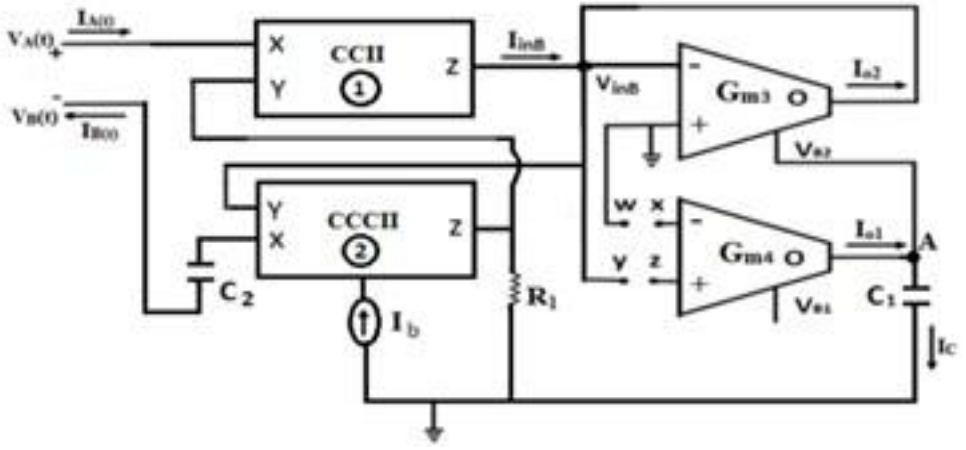


Figure 8. Schematic diagram of floating meminductor emulator

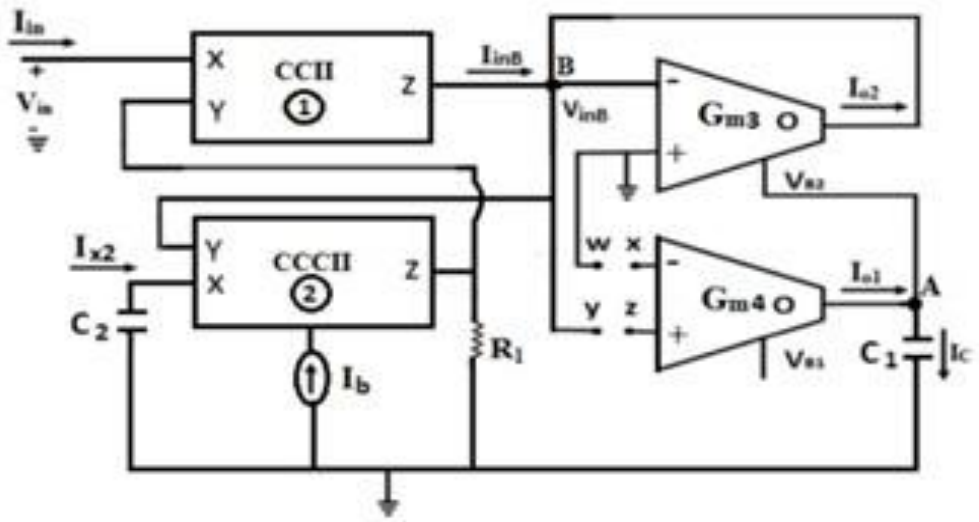


Figure 9. Schematic diagram of grounded meminductor emulator

2.9 Mem-Elements Emulator Design with Experimental Validation and Its Application, Niranjan Raj, et.al. (2021) [14]

study conducted an emulator circuit of mem-elements—memristors, memcapacitors, and meminductors was published in this research. The circuit was implemented utilizing the current mode approach, which outperforms its voltage mode equivalents. A few passive components and current mode analog building blocks were used in the circuit design that has been provided in Fig. 10. Both the simulation and practical data have shown the fingerprint features, which supports the theoretical analysis. Numerous analyses, including process corner, temperature, and non-volatility behavior, have corroborated the design's resilience. The 0.18 μm TSMC process parameter and ±1.2 V power supply were utilized for simulating the mem-elements emulator design. The suggested mem-elements concept is experimentally shown by creating a prototype on a breadboard using the commercial ICs AD844 and CA3080. The meminductor circuit, memristor circuit, and memcapacitor circuit each need a layout area of 8061 μm2, 4829 μm2, and 8098 μm2 square pixels, respectively. It also supplies the electricity that the mem-elements circuit uses. Using mem-elements, a chaos has been developed to demonstrate the emulator's effectiveness.

$$L_M^{-1}(\varphi(t)) = \left(\frac{\alpha_1\alpha_2\beta_1\beta_2\rho(t)}{R_{eq1}R_{eq2}C_{eq1}C_{eq2}} - V_{SS} - 2V_{th}\right) \times \frac{k\alpha_1\beta_1\gamma_2}{\sqrt{2R_{eq1}C_{eq1}}} \quad (24)$$

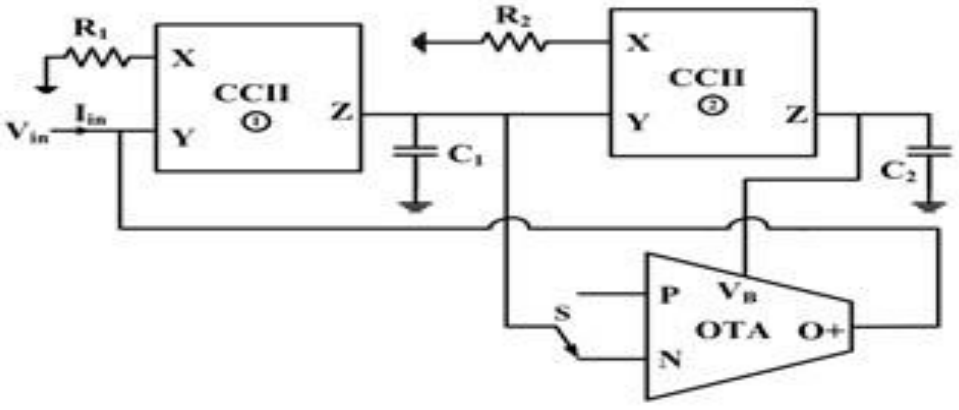


Figure 10. Flux-controlled meminductor emulator circuit design

2.10 VDCC-Based Memcapacitor/Meminductor Emulator and Its Application in Adaptive Learning Circuit, Aneet Singh, et.al. (2021) [11]

study conducted memristor, grounded capacitor, voltage differencing current conveyor, and floating memcapacitor/meminductor emulators. Simply switching the memristor and capacitor locations yields the meminductor emulator, and vice versa. When compared to the majority of designs seen in the literature, the memcapacitor and meminductor emulators that have been presented are quite simplistic. Not only do the suggested emulators pass the non-volatility test, but they also work well throughout a broad frequency range. By including the memristor emulator circuit and the SPICE model of the memristor, the performance of the suggested memcapacitor and meminductor emulators has been confirmed. It turns out that the suggested emulators work fine in both scenarios. Using the specifications of the 0.18 m CMOS technology, the LTspice program has been used to model the suggested architectures. Additionally, suggested memcapacitor and meminductor emulators have been used to create adaptive learning circuits, ensuring the idea's complete viability.

$$M_L = \frac{RC_1C_2}{G_mK\phi_1}\left[1 - \frac{RC_2(V_{ss}+V_{th})}{\phi_1}\right]^{-1} \quad (24)$$

It can be concluded from Eq. (24) that the meminductance of meminductor emulator depends on the values of flux (U1), resistor (R) and the value of capacitor (C2) used in the memristor emulator. It also depends on the value of the capacitor (C1) used in the meminductor emulator shown in Fig. 11.

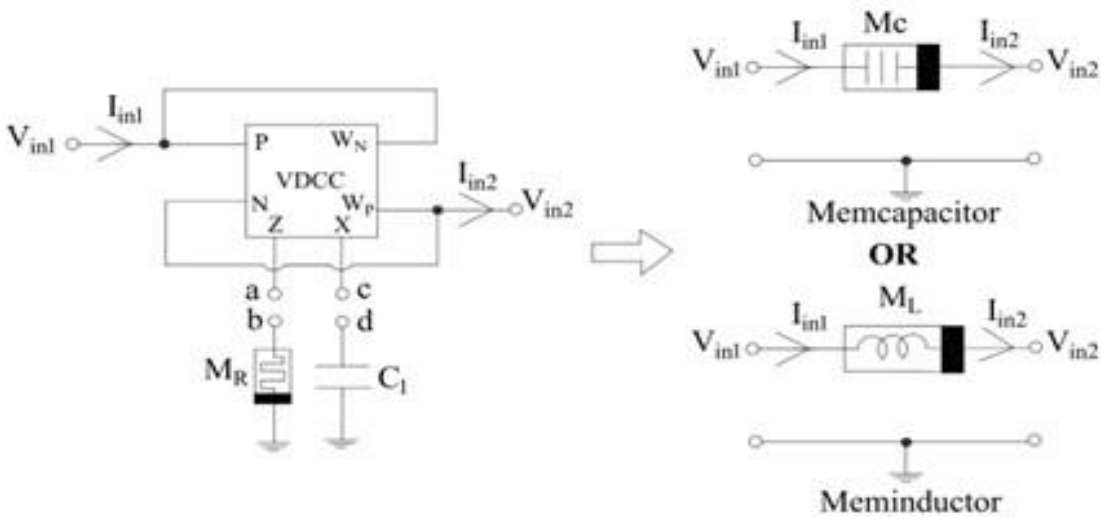


Figure 11. Memcapacitor and meminductor emulators

2.11 Memcapacitor and meminductor circuit emulators: A review, Francisco J. Romero, et.al. (2021) [12]

study conducted Theoretically, a novel circuit element was developed by Prof. L. Chua in 1971 that differed in behavior from the three known passive elements—the resistor, the capacitor, and the inductor [30, 31]. Because its properties were similar to those of a memory resistor, this element was named memristor. The formulation of the constitutive equations of memcapacitors and meminductors, forty years later, expanded the idea of mem-elements to include the other two circuit elements. Many researchers have been interested in developing various uses for these devices since then because to their non-volatile and non-linear features. To study and apply memcapacitors and meminductors in real-world applications, however, circuit emulators are required due to the absence of solid-state implementations of these components. To that end, this study compiles the most prominent alternatives to memcapacitors and meminductors that have recently appeared in the literature. There has been much research and

comparison of many circuit emulators, yielding numerous potential strategies for incorporating these devices into future designs.

2.12 Simple Grounded Meminductor Emulator using Transconductance Amplifier., Ankur Singh, et.al. (2021) [13]

This study describes a grounded meminductor emulator setup where an operational transconductance amplifier (OTA) acts as the central component. Like a pinched hysteresis loop in a perfect meminductor simulator, the circuit has its unique signature. By manipulating the transconductance amplifier's bias voltage, which impacts the transconductance gain, the grounded meminductor architecture may be electrically regulated to alter its properties, allowing it to be managed from outside the device. The suggested meminductor emulator's efficiency has been tested using the Cadence Virtuoso tool and 90nm Complementary Metal Oxide Semiconductor (CMOS) technology.

By changing the switch connection can get decremental/incremental meminductor is obtained final equation as:

$$M^{-1} = \frac{I_{in}(t)}{\phi(t)} = \frac{Kg_{m3}}{C_1}\left(V_{sx} + V_t - \frac{g_{m2}g_{m3}\rho(t)}{C_1C_2}\right) \quad (25)$$

It can be observed from the above equation that the design shown in Fig. 12 shows the decremental meminductor emulator who's initial meminductance value is [((K1gm3)/C1)(Vss+Vt)], and the rate of change of inductance is confirmed by [(K1gm2gm3)/(C].

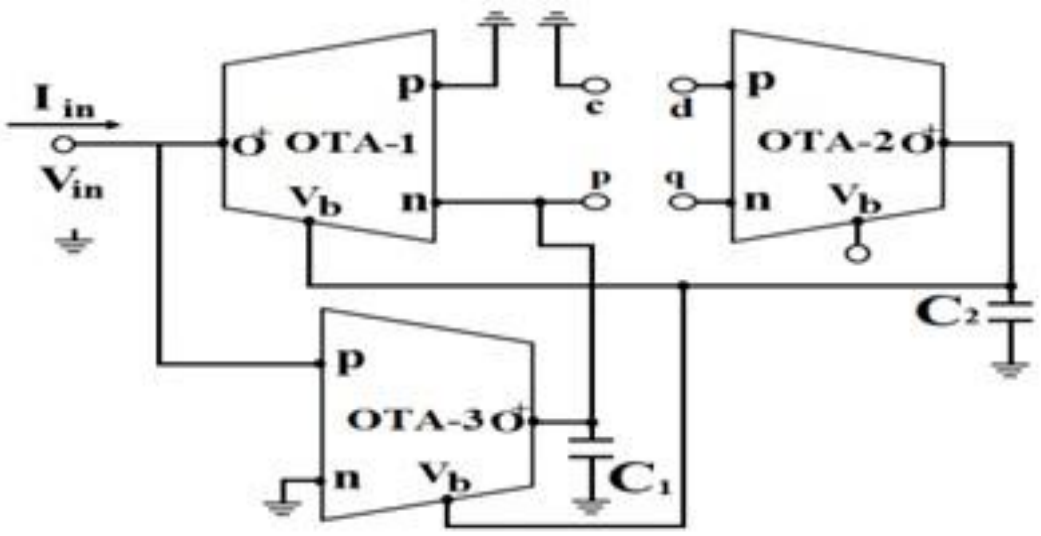


Figure 12. Schematic design of grounded meminductor emulator

2.13 The Simple Charge-Controlled Grounded/Floating Mem-Element Emulator, Yeu Liu, et.al. (2021) [24]

study conducted with each kind of memory element further subdivided into grounded and floating forms, this short proposes a simple charge-controlled emulator for producing all three types. A function of first order polynomial represents all the mathematical models. By connecting three switches (S1/S3) and preserving positions (P1 ~ P3), the memristor (MR), memcapacitor (MC), and meminductor (ML) may be constructed. Up to this point, this is the most basic emulator that can handle the highest operating frequency and largest bandwidth. In particular, the

floating ML emulator's frequency is more than 1.5 MHz. Assuming it lays the groundwork for the next generation of intelligent and neuromorphic computers, the suggested emulator can be set up using a number of commercially available components and used to design integrated circuits with high density, high speed, low power, non-volatility, and good scalability.

$$L_M = \frac{\varphi_{AB}}{i_{AB}} = \frac{R^2 C_2}{10 R_1 C_1}\left(\frac{R_4 R_6}{R_3} - \frac{R_7}{R_5}\right) q_{AB} + R_x\left(\frac{R_4}{R_2} - \frac{R_7}{R_6}\right) \quad (26)$$

When S2 connects to P2 (i.e., an integrator module, see Fig. 13, and P1 is a resistor Rx, the emulator becomes an ML Where, R2, R4 ,R8 ,R7 ,R3 These represent resistors in the circuit. C1 , C2 These are capacitors in the circuit.

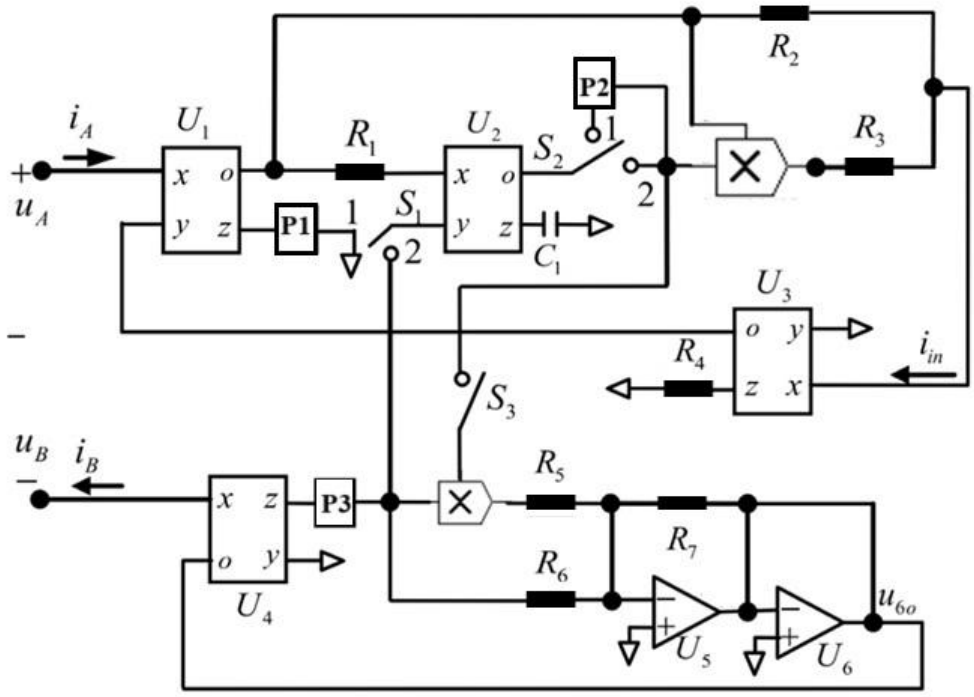


Figure 13. Schematic diagram for memory emulator

2.14 New high frequency memristorless and resistorless meminductor emulators using OTA and CDBA, Nisha Yadav, et.al. (2021) [15]

An existing disparity New meminductor emulators in this study are based on operational transconductance amplifiers (OTAs), two grounded capacitors, and a buffered amplifier (CDBA). Even though the emulators don't use memristors and resistors, almost all of the meminductor emulators found in published works do. The emulators are designed for grounded & floating meminductors with decremental and incremental topologies, respectively shown in Fig. 14 and Fig. 15. The suggested emulators' operating frequencies are raised to 2 MHz for both the grounded and floating versions. Since the transconductance gain controls the generated flux, the circuits are electrically tunable. We finished the Monte Carlo and temperature analyses, and they were both found to be satisfactory. The Eldo simulation tool from Mentor Graphics was used in conjunction with the technology specifications for 180 nm CMOS to get the simulation outcomes. Integrating the suggested meminductor emulator into the construction of ad hoc learning circuits proved its efficacy.

$$M_L = \underbrace{\frac{2C_1}{(\mu_n C_{ox})^2 (V_{SS}+2V_{th})^2}}_{\textit{Fixed part}} + \underbrace{\frac{2C_1 \varphi_{in}\left[\frac{\mu_n C_{ox}\varphi_{in}}{2C_2}-\sqrt{2}\right]}{\mu_n C_{ox} C_2 (V_{SS}+2V_{th})^2}}_{\textit{Variable part}} \quad (27)$$

Cox is related to the capacitance of the gate. Vss is the source voltage and Vth is the threshold voltage. C1 , C2 are the capacitances in the circuit.

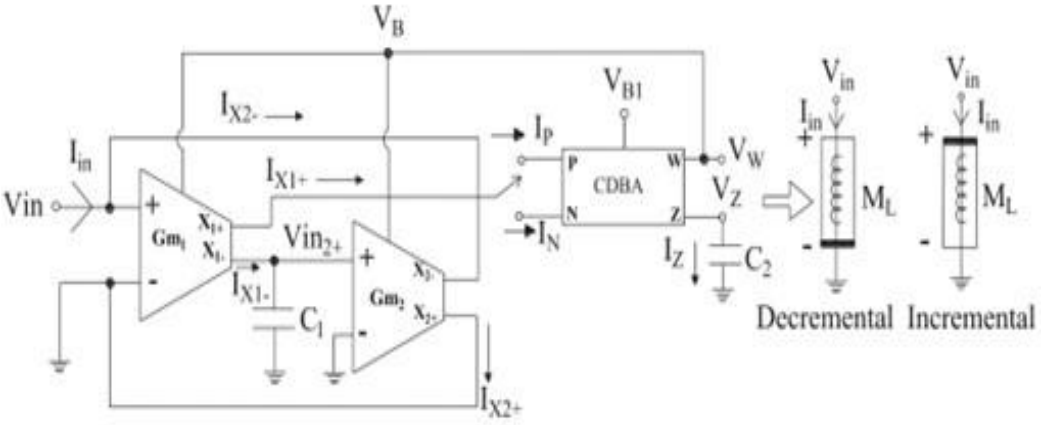


Figure 14. Grounded meminductor emulator

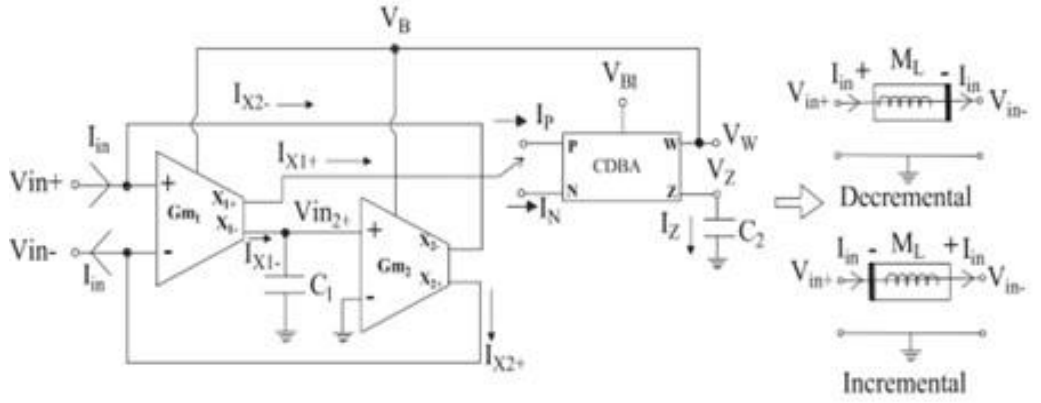


Figure 15. Floating meminductor emulator

2.15 A Flux Controlled MOS-Based Optimized High Frequency Meminductor Emulator, Ananda Y. R, et.al. (2022) [16]

An enhanced meminductor emulator for high-frequency calculations is presented in this study. The meminductor emulator is the initial of its kind to be built using just MOS transistors, opening the door to the fabrication of monolithic integrated circuits. Using Cadence Virtuoso and TSMC 180 nm PDKs, the meminductor is statistically studied, and its operation is validated concerning multiple variables, including process corner changes, voltage, & frequency. Physical testing and post-layout assessment additionally serve to validate the design. The meminductor uses 2350.67 μm2 of area and consumes 3.3 mW. The device outperforms similar current semiconductors in terms of area utilization, highest operating frequency, and power consumption, and it has an ultimate operational frequency of 20 MHz. Additionally, it is 3.42 times, 2 times, and 258 times more efficient. Additionally, by creating a chaotic oscillator to show its usefulness in many different contexts, the meminductor is shown in Fig. 16 to be applicable.

$$\boldsymbol{a} = \frac{K_{M1} g_{m2}^2 g_{m3}}{C_{Mc1} C_{Mc2}} \tag{28}$$

$$\boldsymbol{\beta} = -(V_{SS} + V_{th}) \frac{K_{M1} g_{m2}}{C_{Mc1}} \tag{29}$$

$$\dot{\boldsymbol{\rho}}(\boldsymbol{t}) = \frac{d\rho(t)}{dt} = \boldsymbol{\varphi}(\boldsymbol{t}) \tag{30}$$

$$\boldsymbol{L_m^{-1}}(\boldsymbol{\rho}(\boldsymbol{t})) = [\boldsymbol{\beta} + \boldsymbol{a}\boldsymbol{\rho}(\boldsymbol{t})] \tag{31}$$

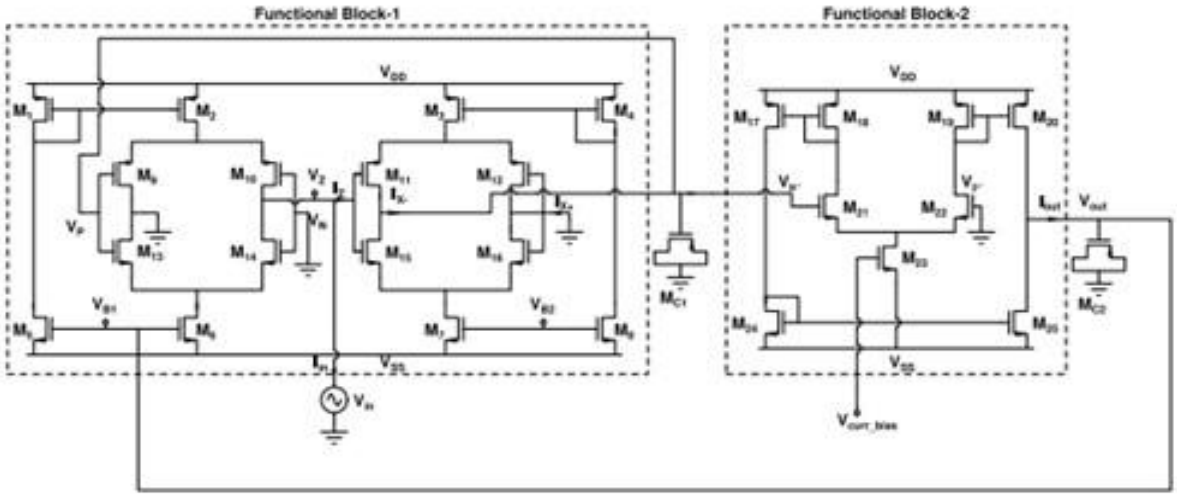


Figure 16. Schematic of meminductor emulator

2.16 A New Electronic Tunable High-Frequency Meminductor Emulator Based on a Single VDTA., Pankaj Kumar Sharma, et.al. (2023) [17]

study conducted using a single voltage difference transconductance amplifier (VDTA), we provide an electrical adjustable grounded meminductor emulator (MIE) in this report. The MIE uses one VDTA, two MOSFETs, and two capacitors. All the suggested MIE only calls for 18 MOS transistors and 2 grounded capacitors. By using Cadence Virtuoso and a 180-nm CMOS library, we were able to verify the suggested MIE's function. Only 1081 μm2 is the layout area of the emulator. This design can function up to 25 MHz. We conducted an experiment utilizing CA3080 ICs to verify the theoretical and simulation findings, and the results confirm the simulation. The total power usage of the suggested layout is 5.93 mW. And the meminductor equation can be expressed as

$$\frac{I_{in}}{\varphi(t)} = \frac{K_1 g_{m2}}{C_1}[-V_{th} - V_{SS}] + \frac{K_1 g_{m0} g_{m2}^2}{C_1^2 C_2} \int \boldsymbol{\varphi}(\boldsymbol{t}) \boldsymbol{dt} \tag{32}$$

Equation (32) has two parts, the first part is the time-invariant part and the second part is the time-variant part. Transconductance gm2 can be tuned by external biasing voltage VB2. Thus, the grounded MIE is electronically tunable is shown in Fig. 17.

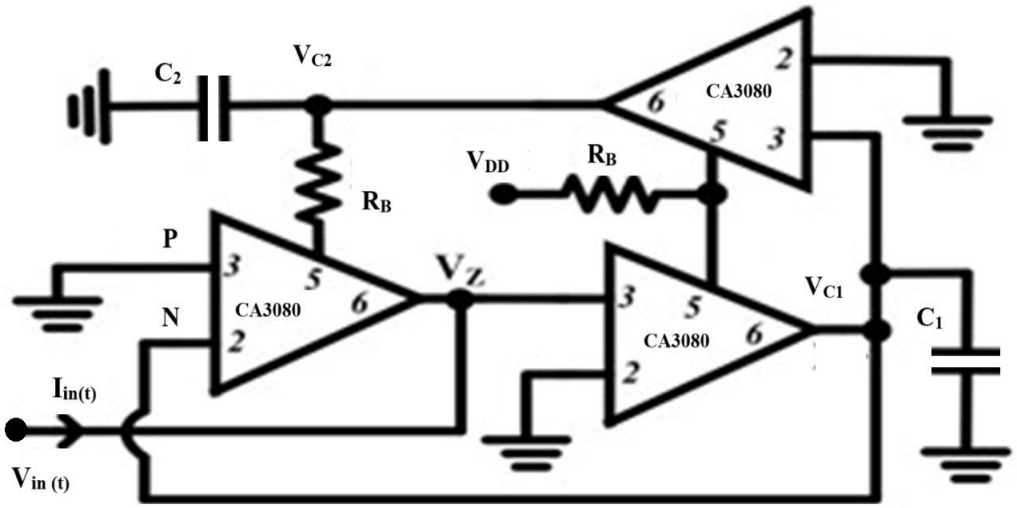


Figure 17. Meminductor Emulator

2.17 Single Active Block-Based Emulators for Electronically Controllable Floating Meminductors and Memcapacitors, Mihajlo Tatovic, et.al. (2023) [19]

Research performed two unique emulator circuits using a single active block are shown in Fig. 18. In order to simulate the operation of a floating, grounded, incremental, or decreasing flux-controlled meminductor, the first circuit makes use of a Voltage Differencing Transconductance Amplifier (VDTA). In the second circuit, which is modeled after a VDCC, the memcapacitance properties are reproduced. There is only one kind of grounded passive element used in both simulation circuits, and that is capacitors. Importantly, these circuits are electrically tunable, so you can tune the inverse meminductance/memcapacitance that really happens. Consideration of possible parasitic effects and non-idealities is a part of the theoretical study of the suggested emulators. These undesirable effects were attempted to be mitigated as much as possible by meticulously choosing the passive circuit components. The suggested circuits are very straightforward when compared to previous designs reported in the literature. Not only that, but they also pass the non-volatility test and show broad frequency operability (up to 50 MHz). Results from simulations employing 0.18 μm CMOS technology and a supply voltage of ±0.9 V closely match the expectations made theoretically. In addition, the circuit's resilience is assessed using Monte Carlo simulations and corner analysis. Experimental testing is conducted utilizing components that are commercially accessible in order to verify the solution's practicality.

$$L_M^{-1}(t) = \pm \frac{\beta_f \beta_s g_{mF} K_s}{C_1} \left[\frac{\beta_f g_{mF} g_{m0}}{C_1 C_2} \rho_{in}(t) - V_{SS} - V_{Tn} \right] \quad (33)$$

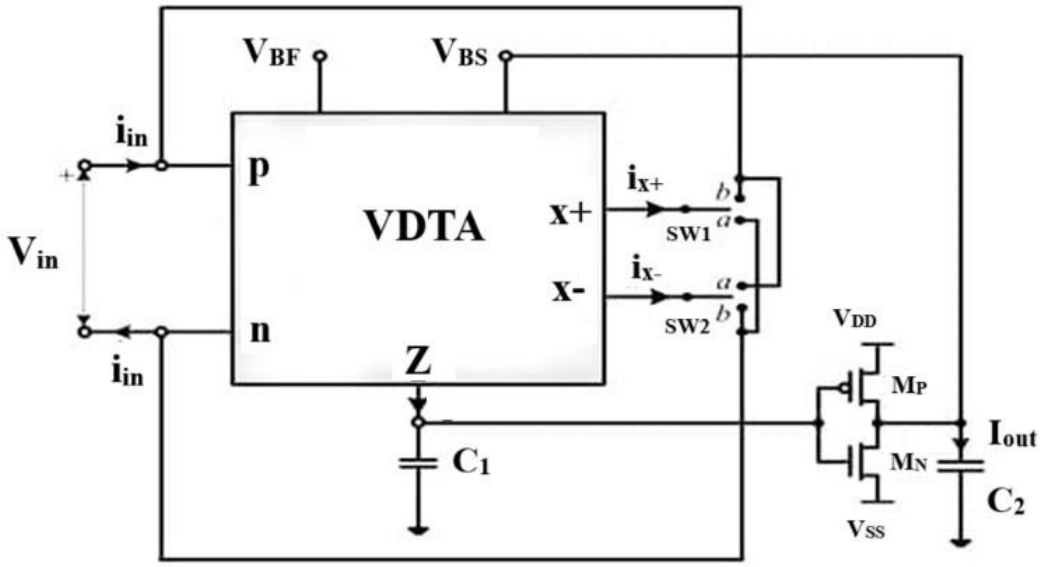


Figure 18. Floating meminductor emulator circuits based on VDTA

2.18 New Modified Voltage Differencing Voltage Transconductance Amplifier (MVDVTA) based Meminductor Emulator and its Applications, Harsh Jain, et.al. (2023) [26]

An innovative meminductor emulator circuit constructed around a modified voltage differencing voltage transconductance amplifier (MVDVTA) is described in this work which is shown in Fig. 19. Simplicity, the use of a single active building block (ABB), and the absence of memristors characterize the emulator circuit. A pair of capacitors and a single resistor are all that are needed for the MVDVTA simulation. A wide frequency range has verified the effectiveness of the concept. With 0.18μm CMOS technology, the LTSpice modeling tool is powered. Circuits designed for use with chaotic oscillators and adaptive learning have also been evaluated to guarantee the operation of the emulator. The design proves its worth in a real-world context since it is efficient enough for both uses. The equivalent meminductor equation is,

$$M_L^{-1} = \frac{1}{C_1 R\sqrt{2}} k(V_{SS} + 2V_{th})\varphi_{in}(t) + \frac{1}{C_1 R\sqrt{2}} k\left(-\frac{g_m}{C_2 C_1 R}\rho_{in}(t)\right)\varphi_{in}(t) \qquad (34)$$

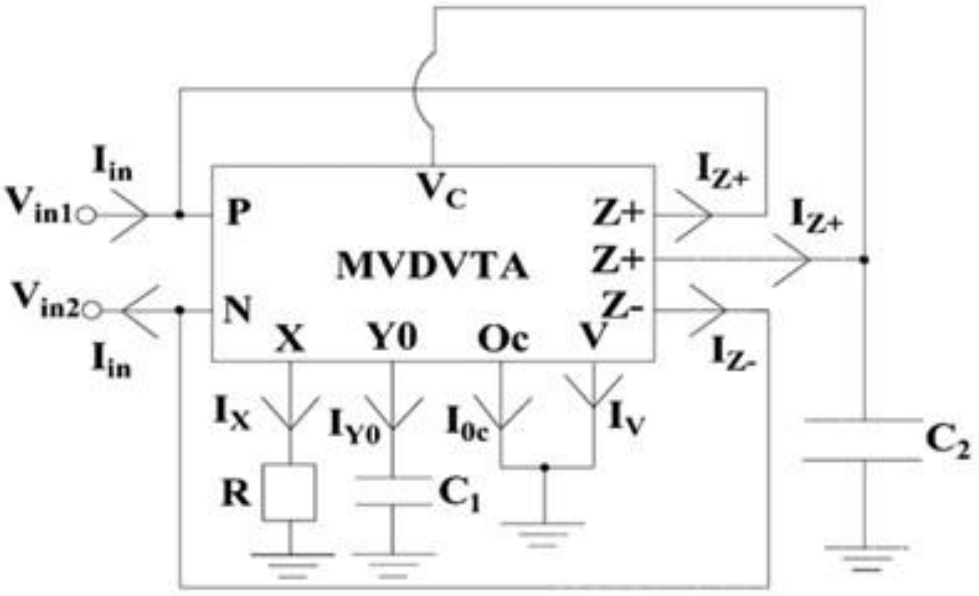


Figure 19. Meminductor emulator circuit diagram

2.19 Electronically Charge-Controlled Tunable Meminductor Emulator Circuit with OTAs and Its Applications, Durmus Ersoy, et.al. (2023) [18]

research performed there has been a recent uptick in research on novel memory-enhancing passive elements like memristors, meminductors, and memcapacitors. This article proposes a meminductor simulator circuit that does not use a memristor but relies on operational transconductance amplifiers (OTAs) shown in Fig. 20. This circuit is compatible with physically produced memristor structures, has charge control, a floating structure, and electronic controllable characteristics. Utilizing 0.18μm CMOS technology, the OTA IC is put to use. Low power consumption and operation in high-frequency zones characterize the meminductor emulator circuit. On top of that, the meminductor emulator circuit works as a rising and a decreasing model. Verifying the resilience of the suggested circuit is done by temperature, Monte Carlo, and worst-case analyses. Using the nonlinearity of the suggested meminductor circuit, a chaotic circuit is built in this work. Furthermore, the memory capability of the suggested meminductor circuit has been shown by the implementation of a neuromorphic circuit. The suggested meminductor circuit's electrical tunability is proven in neuromorphic and chaotic contexts. Electronic models of the suggested meminductor emulator circuit's functionalities, generated using the LTspice software. In this paper meminductance will be obtained by,

$$L_M(q) = \frac{C_1}{g_{m1}g_{m2}} + \frac{C_1 R_1 q}{g_{m1} C_2} \tag{35}$$

Where, LM (q) represents the meminductance as a function of charge, C1 , C2 are capacitors in the circuit.gm1g{m1}gm1 , gm2g_{m2}gm2 are the transconductance parameters of the transconductance amplifiers or OTAs in the circuit. R1 is a resistor in the circuit. q is the charge, which is the integral of current over time.

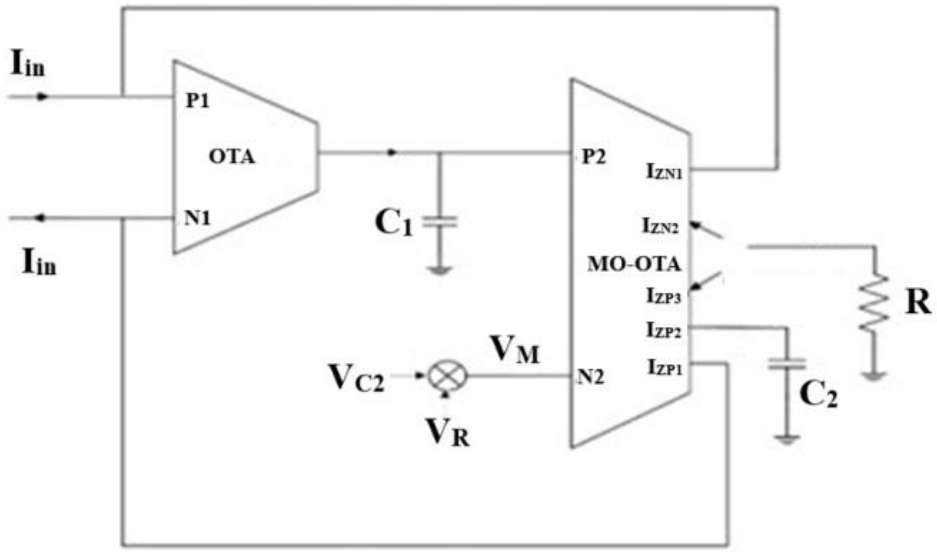


Figure 20. Meminductor emulator circuit based OTAs

2.20 Physical evidence of meminductance in a passive, two-terminal circuit element, Abhiram Dinavahi, et.al. (2023) [20]

studies conducted in the years leading up to the 2019 physical generation of the memcapacitor and the 2008 physical construction of the first purposeful memristor, the development of a meminductor remains unproven. It is in this two-terminal passive system, primarily made up of an electromagnet connected with two permanent magnets, that the first experimental proof of mem inductance arrives. We examine series resistance in detail and see how it stifles our ability to identify possible meminductive processes in physical systems. By treating parasite resistance as a "resistive flux" and discovering a means to eliminate it, we are able to eradicate meminductance from these systems. We prove that mem inductance is an expression of a basic circuit element by laying out its overall origin. Following its lineage from memristors to meminductors explains its position on the electrical circuit elements table; this element has all three of these characteristics.

2.21 A Compact Electronically Tunable Meminductor Emulator Model and Its Application. Pankaj Kumar Sharma, et.al. (2024) [22]

Meminductor emulator with non-ideality shown in Fig. 21 with that study conducted high operational frequency and low power operation are achieved using a tiny MOSFET-C floating/grounded meminductor emulator (MIE) device. With only 22 MOSFETs and 2 capacitors, the MIE that has been presented is very efficient. The Cadence Virtuoso software and hardware prototypes are used for thorough theoretical analysis and performance verification. The suggested MIE efficiently functions throughout a broad frequency range of up to 5 MHz, consumes 590 μW of power at a 180nm CMOS technology node, and displays significant signature qualities. Using 180 nm CMOS technology, the MIE layout area is 13107.5 μm}. Extensive Monte Carlo simulations have been conducted to show that the MIE is resilient, and to examine the implications of MIE element statistical fluctuations. The hardware prototypes have been constructed and tested to validate the experiments. The presentation of a MIE-based adaptive learning neuromorphic circuit demonstrates its ability to imitate the behavioral reactions of amoebas in response to changes in the environment, including temperature.

$$\frac{I_{in}}{\varphi(t)} = \frac{Kg_{m1}}{C_1}[-V_{th} - V_{SS}] - \frac{K_A g_{m2} g_{m1}^2}{\omega^2 C_1^2 C_2} \sin \omega t \quad (36)$$

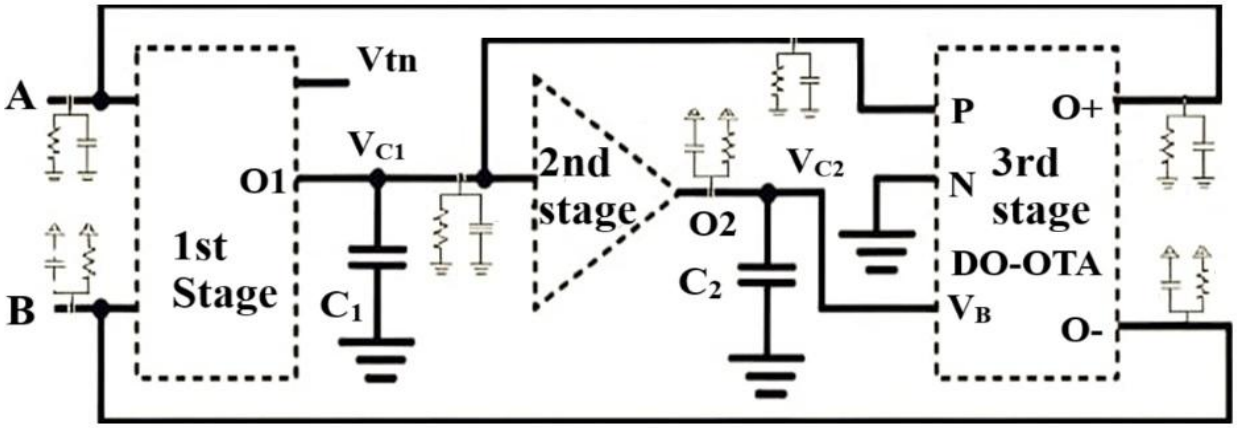


Figure 21. Meminductor emulator with non-ideality

2.22 A new DXCCDITA based meminductor emulator and its application in chaotic oscillator, Bhawna Aggarwal, et.al. (2024) [21]

This study presents a novel meminductor emulator based on a dual-X current conveyor differential input transconductance amplifier (DXCCDITA), its circuit shown in Fig. 22, and it also discusses its use in a chaotic oscillator. It takes one DXCCDITA, two resistors, and two capacitors to make the meminductor emulator a reality. In both decremental and incremental topologies, pinched hysteresis loops are realized throughout a large frequency range, from 100 Hz to 1.5 MHz. Also, the suggested circuit has a toggle that lets you choose between incremental and decremental setups. The effectiveness of the given emulator is clearly shown by analyzing nonvolatility and transient responses. Implementing a chaotic oscillator further validates the circuit's effectiveness, producing results that align with the theoretical framework.

$$M_L^{-1} = -\frac{k}{R_1 C_2 \sqrt{2}} \left(\frac{g_m}{C_1} \varphi(t) - V_{SS} - 2V_{th} \right) \quad (37)$$

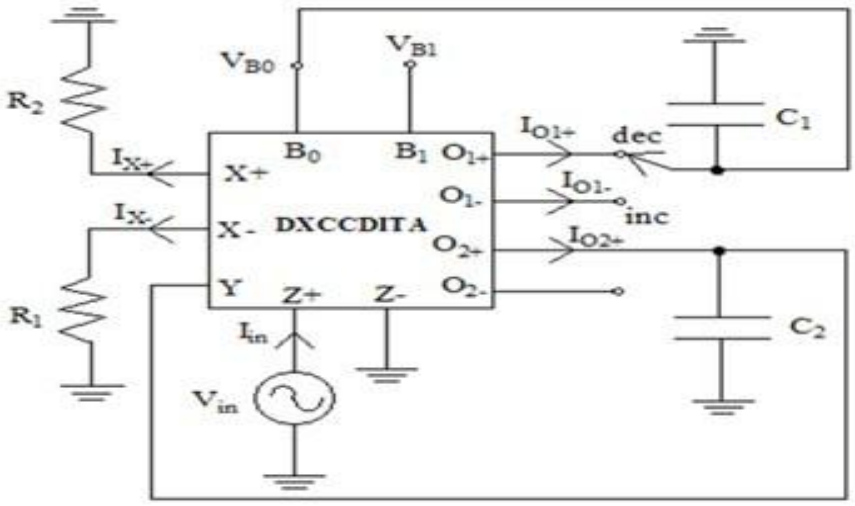


Figure 22. Complete circuit of the DXCCDITA based design of emulator

2.23 High-Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and Application, Garima Shukla, et.al. (2023) [29]

This study introduces a novel method for building anchoring and floating meminductor simulators using two operational transconductance amplifiers (OTAs) and two second-generation present conveyors shown in Fig. 23. It is claimed that the circuits might be used in incremental & decremental designs and are much easier to construct; grounded and floating emulators are also suggested. To test how well the circuits worked, we used Cadence Virtuoso Spectre in addition to standard CMOS 180nm technology. Additionally, they have simulated the suggested circuits after layout and constructed them. The Monte Carlo and non-ideal testing were performed with great care. The use of a meminductor as an AM is also recommended by this research. Results from experiments corroborate theoretical and computational investigations of meminductor emulator circuits.

$$L_M^{-1} = \frac{\varphi_{in}}{I_{in}} \approx \frac{k}{\sqrt{2}R_1C_2}(V_{SS} + 2V_{th}) \pm \frac{k}{\sqrt{2}}\left(\frac{g_{m4}\varphi_{in}}{sC_1R_1^2C_2^2}\right) \quad (38)$$

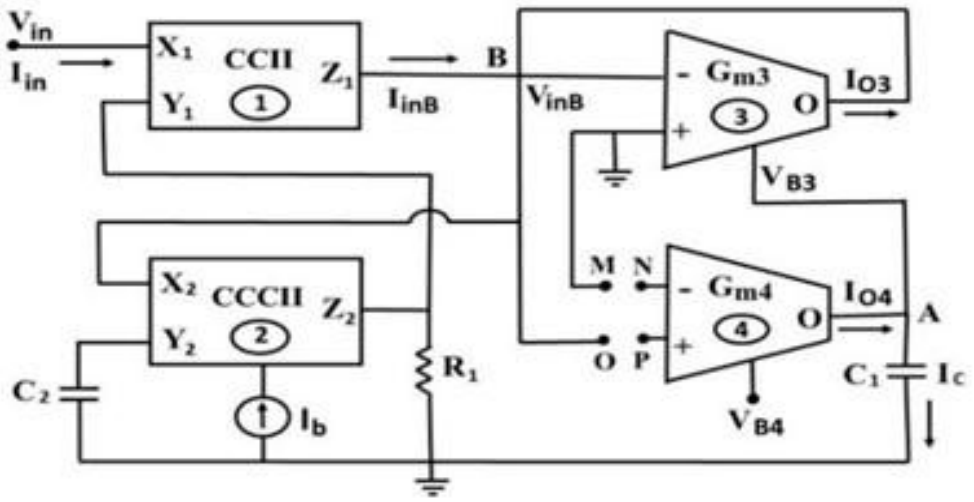


Figure 23. Schematic diagram of grounded meminductor emulator

2.24 Single Operational Amplifier Based Grounded Meminductor Emulator & Its Applications, Hari Om, et.al. (2024) [27]

study conducted simply switching the memristor and capacitor locations yields an emulator that mimics a meminductor, and vice versa. They built two emulators using a single operational amplifier, three resistors, two capacitors, and one component shown in Fig. 24. Equipped with "one operational amplifier, two memristors, two resistors, and two capacitors," the third simulation device was constructed. The suggested circuits for meminductor emulators use hp memristors operating at 500 kHz. The meminductor emulators have good performance across a broad frequency range. We used LTspice to build and test the meminductor emulators. An experimental oscillator was created to evaluate the functionality of a 500 KHz meminductor emulator. Made use of the suggested microcontroller simulator to build and test a high pass filter. To demonstrate the concept's efficacy, a chaotic oscillator was built using a meminductor emulator. Where VSS is the negative supply voltage and Vth is the transistor's threshold voltage, k represents the technology parameters of the MOSFETs forming differential pairs in the transconductance amplifier stage of the block, gm is the transconductance. considering the relation between current and flux Φ(t), ML $^{-1}$ of the suggested topology in decremental configuration can be expressed as,

$$M_L^{-1} = -\frac{k}{R_1C_2\sqrt{2}}\left(\frac{g_m}{C_1}\varphi(t) - V_{SS} - 2V_{th}\right) \quad (39)$$

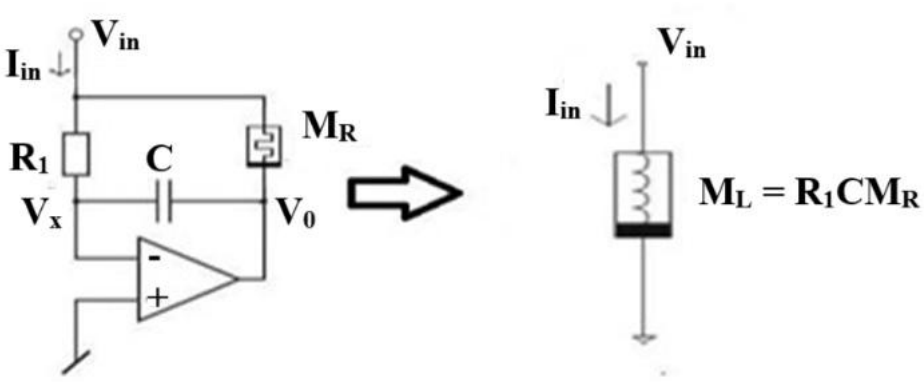


Figure 24. Meminductor emulator circuits

2.25 Grounded Meminductor Emulator using a Single Active Building Block and Its Application., Ankush Choudhary, et.al. (2024) [28]

This construction is an insulated meminductor emulator that combines a grounded memristor emulator, a capacitor, and a dual-X current conveyor differential input transconductance amplifier (DXCCDITA). Several construction components are rendered unnecessary by a single DXCCDITA unit, thanks to its intrinsic electrical tunability. A comprehensive examination of a wide range of frequencies verified the circuit's functionality. For the testing, the LTspice tool and a framework for complementary metal-oxide-semiconductor technology were used, which has a wavelength of 0.18 μm. Additionally, a chaotic oscillator is built as a result of using the suggested module emulator. After extensive testing across all circuit components, the meminductor emulator has shown to be invaluable in practical application. In this research, by using a DXCCDITA block shown in Fig. 25, and its matrix researcher derived impedance of memristor,

$$\boldsymbol{M_R(s)} = \frac{1}{k\left(v_{c_2} - v_{in} - v_{tp}\right)} + \frac{R}{1+sRC_2} \tag{40}$$

From the above equation, the impedance is dependent on the voltages across capacitor C2 and resistor R. the input has been applied to the Y port of the active block, Vy =Vin.

$$\boldsymbol{M_L} = \frac{sC_1 M_R}{g_m} \tag{41}$$

$$\boldsymbol{M_L} = \frac{sC_1}{k\left(v_{c_2} - v_{in} - v_{tp}\right)g_m} + \frac{sC_1 R}{(1+sRC_2)g_m} \tag{42}$$

It is evident that the meminductance is contingent upon both the capacitance (C2) of the capacitor within the memristor emulator and the transconductance (gm) of the DXCCDITA active block.

$k = \frac{\mu C_\alpha W}{2L}$, Where the transconductance parameter k, and W is the effective channel width, L is the effective length of the channel, Cox is the gate oxide capacitance per unit area, and μ the carrier mobility.

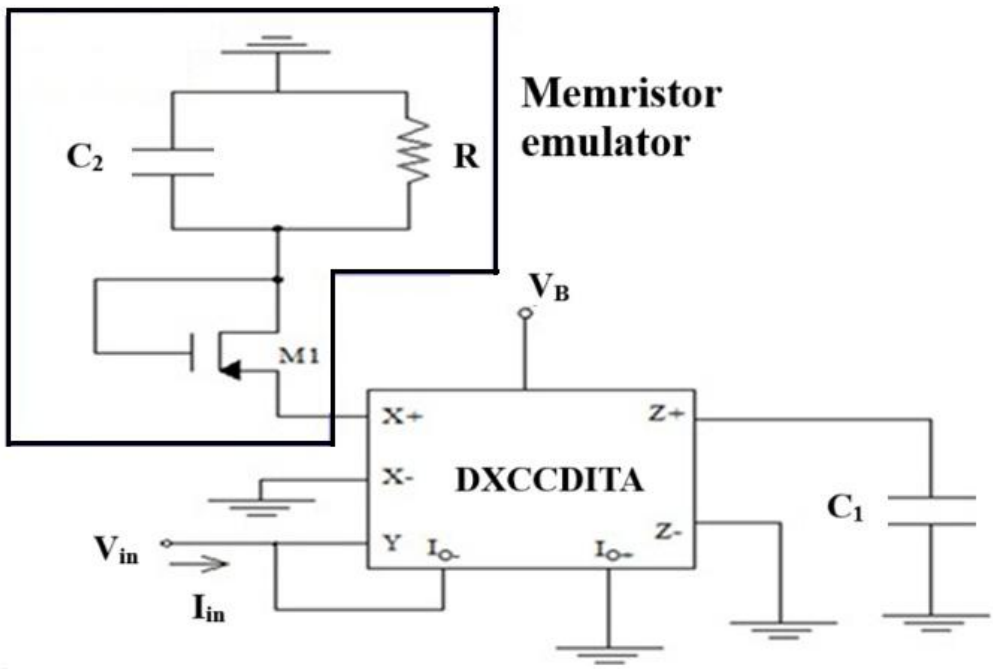


Figure 25. Schematic diagram of grounded meminductor emulator

COMPARATIVE TABLE

The comparative design of meminductor and related design as shown in Table 1.

Table 1. Comparative Analysis of Meminductor and Related Designs.

Ref.	Year	Active Elements	Passive elements	Using Memristor	Using Multiplier	Mode Decremental /Incremental /Both	Supply voltage	Operating frequency	Technology Used	Applications
[1]	1971	Active circuits (operational models using mutators)	Nonlinear resistor, inductor, or capacitor	Yes	No	-	-	-	-	Device modeling, signal processing (e.g. staircase waveform generation)
[3]	2011	four single output second generation current conveyo	resistor, inductor, capacitor	Yes	No	-	-	-	-	use in electronic applications

		rs (CCII+)								
[4]	2014	Current Conveyors (CCII+)	Resistors, capacitors	Yes	No	-	±5V	100Hz-800Hz	PSPICE circuit simulations	Meminductor emulation
[5]	2016	Operational amplifiers, Multipliers	Resistor,capacitor	No	Yes	-	±15V	30Hz-180Hz	multisim simulations	Chaotic oscillator design, meminductor emulation
[6]	2020	Operational amplifiers	Resistors, capacitors, varactor diode	No	No	-	-	4kHz-22kHz	multisim simulations	Transformation among memristor, memcapacitor, and meminductor emulations
[11]	2021	1 Voltage Differencing Current Conveyor(VDCC)	Capacitors	Yes	No	-	± 0.9V	700 kHz	LTspice tool withTSMC 180nmCMOS	Adaptive learning circuits
[13]	2021	Operational Transconductance Amplifiers (OTAs)	Capacitors	No	No	Incremental and decremental	VDD= 1.2V, VSS=-0.5V	100 kHz	90nm CMOS	Meminductor emulation, filters, quadrature oscillators, neuromorphic circuits
[14]	2021	CCII, OTA	2R,2C	No	No	Both	±1.2V(simulation)13, ±15V(experi	Up to 800 kHz (simulation), 2 MHz	0.18 m TSMC process parameter	Chaotic circuits

							mental)	(experimental)		
[16]	2021	MOSFETs only (27)	Two MOS capacitors	No	No	Both	1.8 V (-0.9V to +0.9V)	20 MHz	TSMC 180nm PDK	Chaotic oscillator, memcomputing, secure communication, cryptography
[17]	2023	Single VDTA, 2 MOSFETs (18 MOS transistors total)	Two grounded capacitors	No	No	Both	1.8 V (-0.9 V to +0.9 V)	25 MHz	180-nm CMOS	Memory systems, filters, oscillators, neuromorphic circuits
[19]	2023	1 VDTA, 2 MOSFETs	Two capacitors	No	No	Both	±0.9 V	50 MHz	NA	NA
[24]	2021	CCIIs	7R, Switches	-	Yes	-	-	High frequency regions exceed 1.5MHz.	mathematical models	-
[26]	2023	Modified voltage differencing voltage transconductance amplifier (MVDVTA)	2 Capacitors, 1 Resistor	No	No	Not specified	Not specified	1 kHz to 500 kHz	NA	chaotic oscillator and adaptive learning
[27]	2024	2 OTAs, 2 Current Conveyors	Not specified	Yes	No	Not specified	+/- 15 V	500kHz	Not Specified	chaotic oscillator

[28]	2024	1 DXCCDITA	1 Memristor, 1 Capacitor	Yes	No	Not specified	Not specified	100 kHz – 2 MHz	CMOS 0.18µm	chaotic oscillator

SIMULATION RESULT

In reference (28) A thorough analysis across a broad frequency range confirmed the circuit's operation. The LTspice tool, which has a wavelength of 0.18 µm, and a framework for complementary metal-oxide-semiconductor technology were employed for the testing. Using the module emulator also results in the construction of a chaotic oscillator. The meminductor emulator has proven to be extremely useful in real-world applications following thorough testing across all circuit components. In this study, a DXCCDITA block was used.

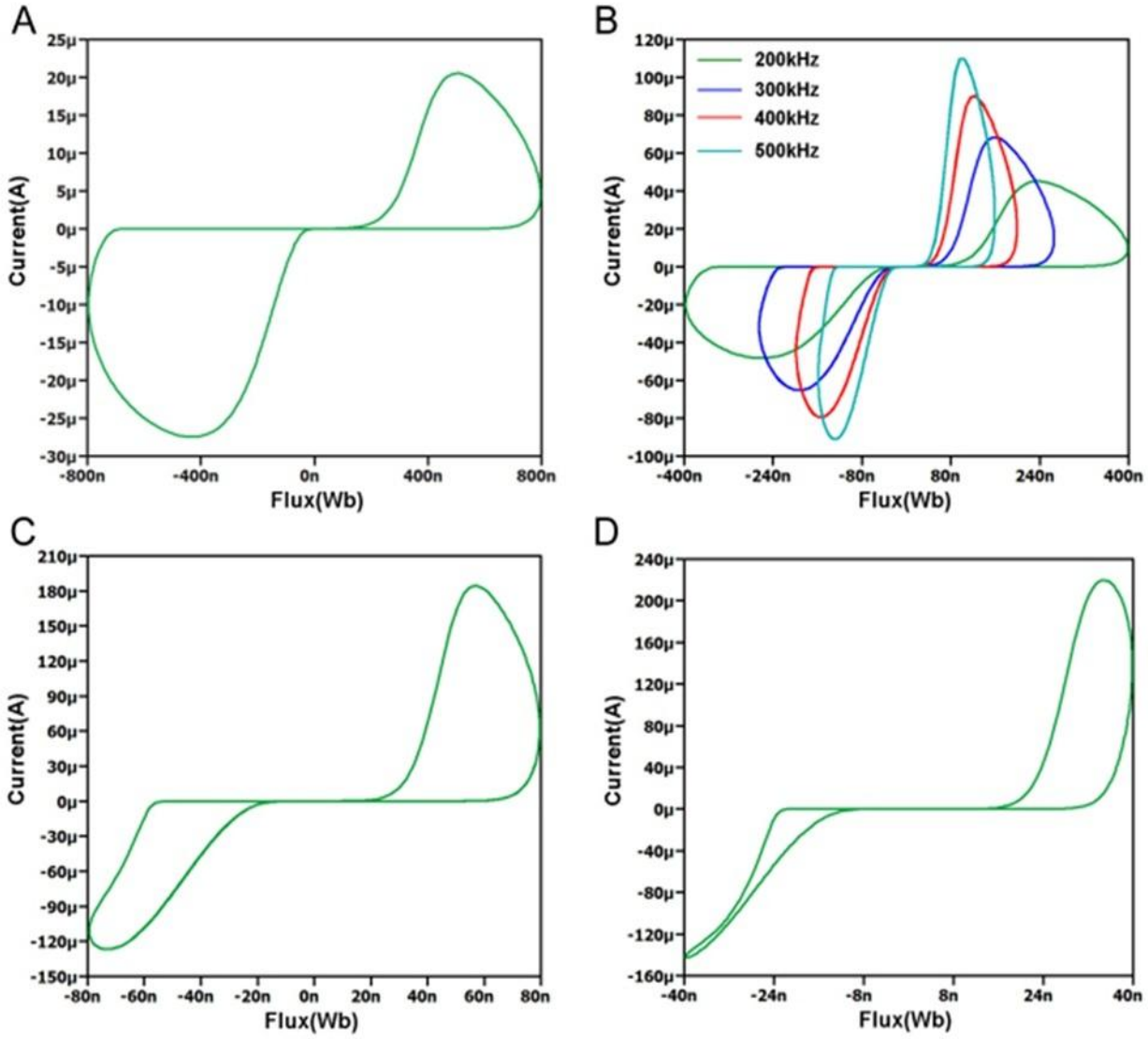


Figure 26. V-I response of the meminductor emulator at different frequencies (a) 100kHz.(b)200 kHz to 500 kHz. (c) 1 MHz. (d) 2 MHz.

RESEARCH GAP

Despite significant advances in the design and implementation of meminductor emulators based on current-mode building blocks, considerable research gaps persist, limiting their popular acceptability and practical application. One significant challenge is achieving flawless replication of meminductive action under shifting operational conditions. Many existing architectures suffer from non-idealities like as parasitic effects and constrained linearity, reducing emulation precision and dependability. Furthermore, scaling remains a significant difficulty, as putting ancient principles into modern integrated circuit (IC) technology is sometimes hampered by high power consumption and complex circuit layout.

Another key difficulty is the lack of set performance benchmarks for comparing various microprocessor emulator architectures. Existing research frequently focuses on particular characteristics such as power efficiency or dynamic range, omitting a thorough examination of the principles. Furthermore, the application-specific flexibility of these emulators is underutilized, particularly in fields such as neuromorphic computing and analog signal processing, where their promise remains untapped. Furthermore, research into how sophisticated current-mode building blocks such as second-generation current conveyors (CCIIs) and integrated circuits (AD844, LT1228, CA3060, etc.) affect emulator performance has only begun. By looking into these gaps, we intend to offer new meminductor emulator designs that are more durable, efficient, and versatile, making them easier to incorporate into real-world applications and cutting-edge technology.

CONCLUSION

This article provides a thorough evaluation of meminductor emulator designs that use current mode building blocks, with a focus on their potential to improve modern electronics. Several studies were successfully conducted, demonstrating a diverse range of circuit architectures and design methodologies aimed at creating exact meminductive behavior. These implementations demonstrated the advantages of current-mode circuits, such as fast operation, low power consumption, and scalability. However, issues such as non-idealities, parasitic effects, and integration restrictions persist, emphasizing the need for further research.

The study also identified key areas for innovation, such as researching better current-mode designs and increasing flexibility to meet application-specific requirements such as neuromorphic systems and reconfigurable circuits. More efficient and adaptable meminductor emulator designs may be conceivable if future research addresses the identified issues. This research is designed to serve as a key resource for academics, guiding the development of next-generation emulators and their inclusion into actual applications.

REFRENCES

[1] Chua, L. (1971). Memristor-the missing circuit element. IEEE Transactions on circuit theory, 18(5), 507-519. https://doi.org/10.1109/TCT.1971.1083337.

[2] Di Ventra, M., Pershin, Y. V., & Chua, L. O. (2009). Circuit elements with memory: memristors, memcapacitors, and meminductors. Proceedings of the IEEE, 97(10), 1717-1724. https://doi.org/10.1109/JPROC.2009.2021077.

[3] Pershin, Y. V., & Di Ventra, M. (2011). Emulation of floating memcapacitors and meminductors using current conveyors. Electronics Letters, 47(4), 243-244. https://doi.org/10.1049/el.2010.7328.

[4] Sah, M. P., Budhathoki, R. K., Yang, C., & Kim, H. (2014, June). A mutator-based meminductor emulator circuit. In 2014 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 2249-2252). IEEE. https://doi.org/10.1109/ISCAS.2014.6865618.

[5] Yuan, F., Wang, G., Jin, P., Wang, X., & Ma, G. (2016). Chaos in a meminductor-based circuit. International Journal of Bifurcation and Chaos, 26(08), 1650130. https://doi.org/10.1142/S0218127416501303.

[6] Yu, D., Zhao, X., Sun, T., Iu, H. H., & Fernando, T. (2019). A simple floating mutator for emulating memristor, memcapacitor, and meminductor. IEEE Transactions on Circuits and Systems II: Express Briefs, 67(7), 1334-1338. https://doi.org/10.1109/TCSII.2019.2936453

[7] Sozen, H., & Cam, U. (2020). A novel floating/grounded meminductor emulator. Journal of Circuits, Systems and Computers, 29(15), 2050247. https://doi.org/10.1142/S0218126620502473

[8] Vista, J., & Ranjan, A. (2019). High frequency meminductor emulator employing VDTA and its application. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 39(10), 2020-2028. https://doi.org/10.1109/TCAD.2019.2950376

[9] Liu, Y., & Iu, H. H. C. (2020). Novel floating and grounded memory interface circuits for constructing mem-elements and their applications. IEEE Access, 8, 114761-114772. https://doi.org/10.1109/ACCESS.2020.3004160

[10] Sharma, V. K., Ansari, M. S., & Parveen, T. (2020). Tunable memristor emulator using off-the-shelf components. Procedia Computer Science, 171, 1064-1073. https://doi.org/10.1016/j.procs.2020.04.114.

[11] Singh, A., & Rai, S. K. (2021). VDCC-based memcapacitor/meminductor emulator and its application in adaptive learning circuit. Iranian Journal of Science and Technology, Transactions of Electrical Engineering, 45, 1151-1163. https://doi.org/10.1007/s40998-021-00440-x.

[12] Romero, F. J., Ohata, A., Toral-Lopez, A., Godoy, A., Morales, D. P., & Rodriguez, N. (2021). Memcapacitor and meminductor circuit emulators: A review. Electronics, 10(11), 1225. https://doi.org/10.3390/electronics10111225.

[13] Singh, A., Borah, S. S., & Ghosh, M. (2021). Simple Grounded Meminductor Emulator using Transconductance Amplifier. Midwest Symposium on Circuits and Systems, 2021-Augus, 1108–1111. https://doi.org/10.1109/MWSCAS47672.2021.9531754.

[14] Raj, N., Ranjan, R. K., Khateb, F., & Kumngern, M. (2021). Mem-Elements Emulator Design with Experimental Validation and Its Application. IEEE Access, 9, 69860–69875. https://doi.org/10.1109/ACCESS.2021.3078189.

[15] Yadav, N., Rai, S. K., & Pandey, R. (2022). New high frequency memristorless and resistorless meminductor emulators using OTA and CDBA. Sādhanā, 47(1), 8. https://doi.org/10.1007/s12046-021-01785-z.

[16] Ananda, Y. R., Satyanarayan, G. S., & Trivedi, G. (2022). A flux controlled MOS-based optimized high frequency meminductor emulator. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 12(4), 774-784. https://doi.org/10.1109/JETCAS.2022.3221305.

[17] Sharma, P. K., Tasneem, S., & Ranjan, R. K. (2023). A new electronic tunable high-frequency meminductor emulator based on a single VDTA. IEEE Canadian Journal of Electrical and Computer Engineering, 46(2), 179-184. https://doi.org/10.1109/ICJECE.2023.3261886.

[18] Ersoy, D., & Kaçar, F. (2023). Electronically charge-controlled tunable meminductor emulator circuit with OTAs and its applications. IEEE Access, 11, 53290-53300. https://doi.org/10.1109/ACCESS.2023.3281200.

[19] TATOVIC, M., & PETROVIC, P. B. (2023). Single Active Block-Based Emulators for Electronically Controllable Floating Meminductors and Memcapacitors. Radioengineering, 32(4). https://doi.org/10.13164/re.2023.0568.

[20] Dinavahi, A., Yamamoto, A., & Harris, H. R. (2023). Physical evidence of meminductance in a passive, two-terminal circuit element. Scientific Reports, 13(1), 1817. https://doi.org/10.1038/s41598-022-24914-y.

[21] AGGARWAL, B., RAI, S. K., & JAIN, H. (2024). A new DXCCDITA based meminductor emulator and its application in chaotic oscillator. Turkish Journal of Electrical Engineering and Computer Sciences, 32(6), 790-805. https://doi.org/10.55730/1300-0632.4103.

[22] Sharma, P. K., Ranjan, R. K., & Kang, S. M. (2024). A Compact Electronically Tunable Meminductor Emulator Model and Its Application. IEEE Circuits and Systems Magazine, 24(3), 8-18. https://doi.org/10.1109/MCAS.2024.3353151.

[23] Shukla, G., Kumar, P., & Paul, S. K. (2023). High -Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and its application as AM Modulator. Informacije MIDEM, 53(3). https://doi.org/10.33180/InfMIDEM2023.303.

[24] Liu, Y., Iu, H. H. C., Guo, Z., & Si, G. (2020). The simple charge-controlled grounded/floating mem-element emulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(6), 2177-2181. https://doi.org/10.1109/TCSII.2020.3041862.

[25] Jain, H., Rai, S. K., & Aggarwal, B. (2023). A new electronically tunable current differencing transconductance amplifier based meminductor emulator and its application. Indian Journal of Engineering and Materials Sciences, 30(4), 550–558. https://doi.org/10.56042/ijems.v30i4.2047.

[26] Jain, H., Aggarwal, B., & Rai, S. K. (2023). New modified voltage differencing voltage transconductance amplifier (MVDVTA) based meminductor emulator and its applications. Indian Journal of Pure & Applied Physics (IJPAP), 61(4), 239-246. https://doi.org/10.56042/ijpap.v61i4.71313.

[27] GUPTA, S., SINGH, K., & RAI, S. K. (2024). A single operational amplifier-based grounded meminductor mutators and their applications. Turkish Journal of Electrical Engineering and Computer Sciences, 32(5), 698-717. https://doi.org/10.52783/jes.3714.

[28] Choudhary, A., Singh, K., Singh, S., & Rai, S. K. (2024). Grounded Meminductor Emulator using a Single Active Building Block and Its Application. Electrica, 24(3). https://doi.org/10.5152/electrica.2024.24050.

[29] Shukla, G., Kumar, P., & Paul, S. K. (2022). High-Frequency Tunable Grounded & Floating Incremental-Decremental Meminductor Emulator and Application. arXiv preprint arXiv:2205.06221. https://doi.org/10.48550/arXiv.2205.06221.

[30] Kushwaha, A. K., & Paul, S. K. (2016). Inductorless realization of Chua's oscillator using DVCCTA. Analog Integrated Circuits and Signal Processing, 88, 137-150. https://doi.org/10.1007/s10470-016-0746-9.

[31] Kushwaha, A. K., & Paul, S. K. (2016). Chua's oscillator using operational transresistance amplifier. Revue Roumaine des Sciences Techniques-Serie Electrotechnique et Energetique, 61(3), 299-303.