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Research Article

Efficient Counter-Driven Linearity Calibration For SHDAC In High-Speed Applications

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ABSTRACT

Achieving both high resolution and high sample rates is a major difficulty in the field of high-speed analog-to-digital conversion for 5G communications. In order to improve speed and resolution, this work presents a novel method that combines an 8-bit Sigma-Delta (ΣΔ) ADC with a 3-bit Flash analog-to-digital converter (ADC). The proposed High-Speed and Sample Hold-Digital-Analog Converter (SHDAC) may operate at sampling frequencies ranging from 1 giga-samples per second (Gsps) to 14 Gsps and across a variety of voltage sampling ranges from 2 to 32 scales. The SHDAC successfully strikes a balance between speed and accuracy by utilizing the high-speed conversion capability of the 3-bit Flash ADC and the oversampling and noise reduction advantages of the 8-bit Sigma-Delta ADC. This makes it ideal for 5G digital communication and signal processing applications. The use of a digital scaling mechanism that dynamically modifies the SHDAC's bit resolution to 4, 8, 16, or 32 bits depending on system requirements is a significant breakthrough in this architecture. Because of its versatility, the SHDAC can be used for a variety of 5G applications, such as high-precision signal processing with lower sample rates and ultra-fast data gathering with lesser resolution. High precision, scalability, and adaptability are ensured by the front-end Verilog model used to implement the suggested SHDAC architecture. The efficiency of the SHDAC is validated by Vivado simulations, which show sampling rates ranging from 1 to 14 Gsps and an ultra-low dynamic power usage of 0.0007w, Sampling rate is 4.286GSpS and SNDR value is 68.98dB, These findings demonstrate how the SHDAC with parasitic capacitance using Counter design with linear correction process for high-speed design can facilitate fast, and to energy-efficient data conversion for upcoming 5G communication systems.

Keywords: *Parasitic capacitance, Linearity correction, Analog to digital converter,*

1.Introduction

However, each architecture serves a distinct function within the broader 5G ecosystem. Because sigma-delta ADCs work well in applications needing high resolution (often 16 bits or more), they are a good fit for several 5G system components that need great dynamic range and low noise. Low Sigma-Delta ADCs are particularly effective in lower-bandwidth applications, such as digital pre-distribution (DPD) or baseband processing, where precision is more crucial than speed.

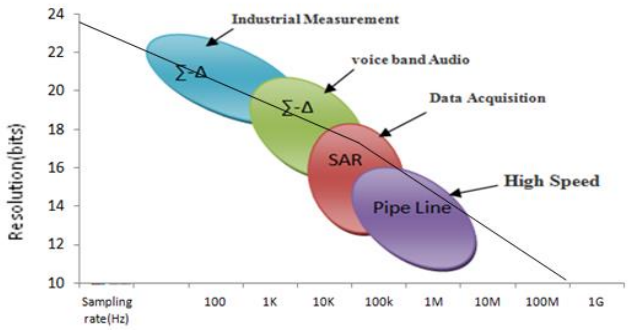

Figure.1 ADC architectures, applications, resolution, and sampling rate

The improvements in CMOS scaling over the last few decades have greatly improved digital circuits due to the downscaling of transistors and the capacity to handle signals at higher frequencies. As a result of the continuous transition to the digital realm, there is a significant need for high performance analog-to-digital

converters (ADCs). The design of conventionally used ADC designs is more difficult, though, because analog circuits do not equally benefit from technological scaling. One kind of ADC that combats this tendency is the Sigma-Delta (SD) ADC, which trades circuit precision against time and is based on oversampling and noise shaping [1]-[4]. Figure.1 shows the approximate sample rate and resolution parameters of three commonly used ADC structures: pipeline, SAR, and delta-sigma. A delta-sigma ADC is used when sampling rates between tens of SPS and several ksps with resolution of 16 bits or more are required, while a SAR ADC is used when power consumption is critical or when sampling rates between several tens of ksps with resolution of 16 bits or less are required.[5]-[8]. High resolution, high speed, and ultra-low power (microwatts) are essential for many wireless receiver system applications. These essential needs can be satisfied by a variety of ADC architectures. To meet these criteria, different architectures are used, depending on the application: pipelined, sigma-delta, flash type, folding, sub ranging, and interleaved techniques. Flash ADC architecture has been demonstrated to be the most efficient of these for applications such as digital storage oscilloscopes, high-speed data acquisition systems, and ultra-wideband (UWB) communication systems. Blue-Ray or DVD readouts, remote sensors, space probes, and advanced video processing systems.

2.Related work

Seong, K et.al [9]-[12], described a high-speed, high-resolution SAR ADC intended for quick sampling uses, like data gathering and high-speed transmission. It achieves a sampling rate of 1.6 GS/s while preserving 12-bit resolution by utilizing a time-interleaved design with numerous concurrent ADC channels. By using a background timing skew calibration technique, the authors tackle the problem of timing skew between channels, which can cause distortion. By boosting linearity and decreasing distortion, this real-time calibration constantly fixes mismatches without the need for outside assistance, improving the spurious-free dynamic range (SFDR) and signal-to-noise ratio (SNR). In comparison to conventional time-interleaved ADCs, the design also incorporates effective power management and digital correction algorithms, which enhance power efficiency and lower consumption. This study combines efficient performance for contemporary high-bandwidth applications with real-time calibration, marking a substantial leap in high-speed ADC design.

Y. Chen et.al. [13], Presented about the high-speed, high-resolution analog-to-digital converter (ADC) "A 14-bit 3 GS/s Hybrid Pipeline-SAR ADC in 16nm CMOS" is intended for applications that demand both high sampling rates and accuracy[14-16]. The authors obtain a 3 GS/s sample rate with 14-bit resolution by combining pipeline and successive approximation register (SAR) designs, which makes it appropriate for data gathering and transmission systems. The hybrid architecture improves speed and accuracy by utilizing the high-speed advantages of the pipeline stage for coarse conversion and the SAR stage for fine resolution. The design is used with 16nm CMOS technology, which provides reduced area and increased power efficiency. The authors incorporate sophisticated calibration procedures to account for mismatches and non-linearities, guaranteeing precise signal conversion, in order to further maximize performance[17,18].

L. Zhang et.al. [19] Presented the high-speed analog-to-digital converter (ADC) "A 10-bit 2.5 GS/s Hybrid SAR-Flash ADC for 5G Applications" was created to satisfy the needs of 5G communication systems, which call for low power consumption and high sampling rates. To attain a 2.5 GS/s sampling rate with 10-bit resolution, the authors suggest a hybrid design that combines Flash ADCs with successive approximation registers (SAR). While the SAR ADC carries out the fine conversion to improve accuracy, the Flash ADC manages the coarse conversion stage, offering quick initial quantization. This combination enables the design to effectively balance resolution and speed. The study also discusses issues with noise reduction and power economy, using calibrating methods to reduce discrepancies and enhance linearity. Because of its low power consumption, the resulting ADC maintains good dynamic performance and precision, making it appropriate for portable and power-constrained 5G devices.

R. Kumar et.al.[20] The high-speed, high-resolution analog-to-digital converter (ADC) described in the paper "A 12-bit 2 GS/s Two-Step ADC with Background Calibration" is intended for applications that need accuracy and quick sampling rates. The advantages of a coarse and fine conversion procedure are combined in the authors' two-step ADC architecture. A Flash ADC performs a coarse quantization in the first stage, offering a quick but imprecise conversion. In order to improve accuracy, the conversion is refined in the second step using a fine-resolution successive approximation register (SAR) ADC. The authors employ a background calibration technique to correct for non-linearities and mismatches brought on by parasitic effects and other flaws. Through constant error monitoring and correction during regular operation, this calibration procedure improves the linearity and lowers distortion of the ADC.

M. Ali et.al. [21] The high-speed analog-to-digital converter (ADC) described in the paper "Design of a 10-bit 4 GS/s Time-Interleaved Hybrid ADC for Ultra-Wideband Applications" is specifically designed for ultra-wideband communication systems. The authors suggest a hybrid architecture that achieves a 4 GS/s sampling rate with 10-bit resolution by combining time-interleaving with a multi-stage conversion method. The effective sampling rate is increased by the design's use of several parallel ADC channels that operate in a time-interleaved fashion. The authors use calibration approaches that adjust for timing skew and gain faults in real time to improve accuracy and reduce channel mismatches. The hybrid architecture improves performance and power economy by utilizing successive approximation register (SAR) ADCs' precision for fine conversion and Flash ADCs' speed for coarse quantization. The structure is appropriate for ultra-

wideband applications, such as radar systems and high-speed data gathering, because to its low power consumption and strong linearity.

3. Proposed Work

3.1Merged Sample-and-Hold and Digital-to-Analog Converter (SHDAC) Circuit

Several crucial steps are involved in the block-level construction of a hybrid ADC system employing a Flash ADC and a Sigma-Delta (ΣΔ) ADC. Each step is intended to accomplish particular goals while guaranteeing the effective operation of the entire system. The Flash ADC, Sigma-Delta ADC, Sample and Hold DAC (SHDAC), Calibration System, and Error Correction/Parasitic Compensation blocks are the essential components of a hybrid system. Every block is essential to the conversion process, allowing for high-speed operation and precise resolution.

3.1.1.Flash ADC

The hybrid system's initial stage is the Flash ADC. Its main job is to use a variety of comparators to convert the input signal at fast speed. These comparators use a collection of reference voltages, usually in the form of a voltage ladder, to compare the input signal to. Eight comparators are needed for a 3-bit resolution, and each comparator produces a binary signal (0 or 1) based on whether the input voltage is higher than the reference value. An encoder block subsequently processes the comparators' outputs, transforming the binary signals into a digital representation. Because of its parallel structure and low number of comparators, the Flash ADC has poor resolution, making it perfect for recording quick transients in the input signal. To increase overall resolution, its coarse quantization is improved by combining it with the Sigma-Delta ADC.

3.1.2. Sigma-Delta ADC

By employing noise shaping techniques and oversampling the signal, the Sigma-Delta ADC block is intended to increase the resolution of the Flash ADC. The Sigma-Delta ADC further processes the remaining or finer details after the Flash ADC records the signal's coarse quantization. The system is driven by a high-speed clock to produce a 1-bit or multi-bit bit stream that represents the input signal after the modulator in the Sigma-Delta ADC integrates the input signal over time. The resolution of the signal is then improved using a decimation filter, which lowers the bit stream's sample rate. The input of a conventional first-order modulator is oversampled at a rate that is far greater than the output rate, and the quantization noise is shaped out of the signal band. By eliminating high-frequency noise, the decimation filter creates a low-speed, high-resolution output that more accurately represents the original signal. This block improves the signal-to-noise ratio and refines the quantization to make up for the Flash ADC's poor resolution.

3.1.3.Sample and Hold DAC (SHDAC)

Because it produces the residue voltage that permits sub-range operation, the SHDAC block is essential to the hybrid system. The input signal and the Flash ADC output are sampled by the SHDAC after the Flash ADC produces a coarse digital output. The residue voltage, which is subsequently stored and sent to the Sigma-Delta ADC for finer quantization, is determined by subtracting these two values. Typically, a switching network and sampling capacitors make up the SHDAC, which regulates when the input is sampled and when residue is produced. This enables the Flash ADC to perform the quick, coarse sampling while the Sigma-Delta ADC handles the high-resolution part of the conversion. By precisely passing the residual signal to the Sigma-Delta ADC, the SHDAC makes it possible for both ADC types to work together to achieve high-speed and high-resolution conversion.

3.2. Error Correction/Parasitic Compensation

Maintaining the hybrid ADC's performance requires error correction and parasitic compensation. Because the comparators in the Flash ADC are susceptible to parasitic capacitances, the timing of the comparator outputs may be distorted, resulting in inaccurate conversion. Furthermore, parasitic capacitances in the modulator or feedback loop of the Sigma-Delta ADC may have an impact, introducing non-linearities and lowering overall performance. In order to counteract these effects and guarantee that the ADC system runs linearly and with little distortion, the error correction block uses compensation techniques. These strategies include linearization techniques like adaptive compensation circuits or calibration algorithms, which dynamically modify the system to account for any parasitic effects. This block is essential for guaranteeing that both ADCs in the hybrid system operate at their best, lowering mistakes and enhancing the ADC's overall efficiency.

The Flash ADC performs high-speed, coarse sampling of the input signal at the beginning of the hybrid ADC's operation. After calculating the residue, the SHDAC receives the output from the Flash ADC and sends it to the Sigma-Delta ADC. The residue is further processed by the Sigma-Delta ADC through noise shaping and oversampling, producing a high-resolution digital output. The calibration and error correction blocks make sure that the Flash and Sigma-Delta ADCs are functioning correctly during this process by making up for any offsets, non-linearities, or parasitic effects that might occur. The hybrid ADC is perfect for applications requiring accurate, quick signal conversion because of the combination of these blocks, which enables it to accomplish both high speed and high resolution. This hybrid ADC system's block-level implementation

provides a thorough method for converting signals at high speeds and high resolutions. Even in demanding high-frequency settings, the system maintains speed and accuracy by fusing the advantages of the Flash ADC and Sigma-Delta ADC.

When it is possible that alternative capacitances could occur, the parasitic capacitance design is crucial to making the necessary modifications to the circuit's design performance. The below flow chart Figure.2 shows the overall Flow Diagram of parasitic integration in SHDAC.

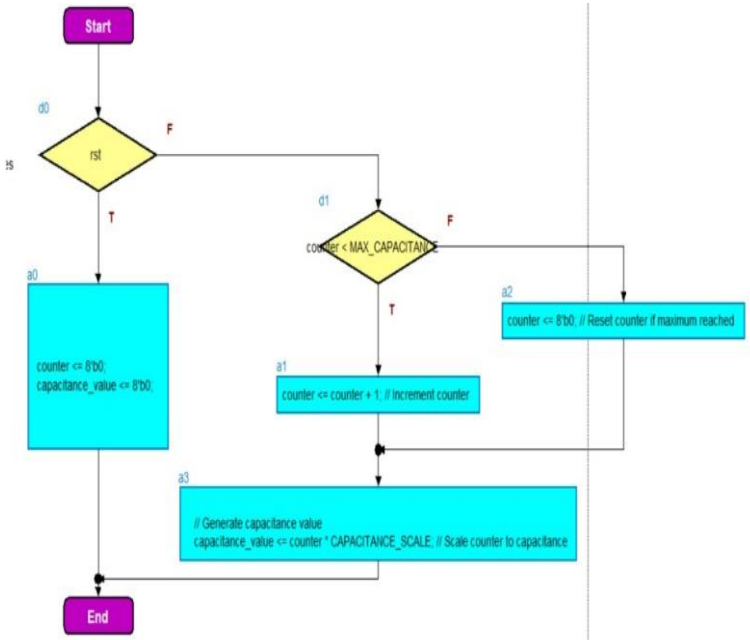

Figure 2. Representing the overall Flow Diagram of parasitic integration in SHDAC

In order to build an interface for the electric field that signifies a charge to be held on each wire as creating a capacitance effect, an electrostatic voltage is created when the results of Flash and Sigma-Delta are combined. This voltage is made up of several bits that are either linked or close together. The primary problem with the current method of reducing the parasitic conditions is a buffer or a register (n-bit) that indicates possible changes on degradation of the signal integrity, causing delays, amplitude attenuations, or peak overshoots, among other factors. Both active and passive parameters for parasitic capacitance are included in the proposed design, along with a delay component for the input's active and passive considerations. Figure 2 above is used to generate the parasitic cap calculation. With clk and rst acting as input parameters to manage the initial states of the capacitance value generated by the frequency of operation of the capacitance type utilized, the general flow diagram for designing parasitic capacitance consists of four steps. This figure reflects the count of the peak value during rising voltage changes when the counter reaches its highest value. Consequently, the capacitance value is given; in the event that the difference is negative, the capacitance value falls in order to reflect the voltage differential.

4.Results and Discussion

The below Figure.3 represents the Main RTL Schematic of parasitic capacitance for the proposed design on hybrid ADC

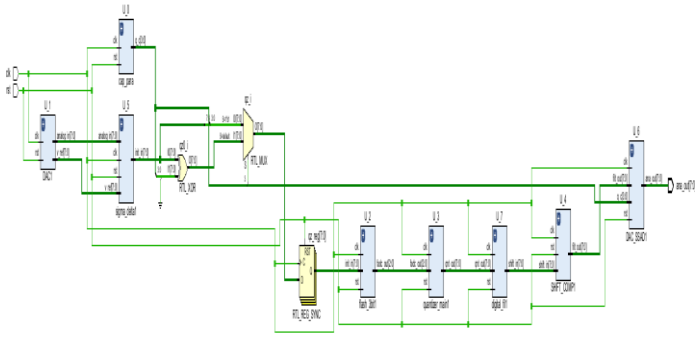

Figure.3.Represents RTL Schematic of parasitic capacitance for the proposed design on hybrid ADC

The RTL schematic diagram of parasitic capacitance on a hybrid ADC is shown in Figure 3. An interface for the electric field that indicates a charge to be stored on each wire as producing a capacitance effect is created by combining the Flash and Sigma-Delta results to create an electrostatic voltage with distinct bits (voltage) outcomes that are either joined or close together. The key problem with current strategy for decreasing the parasitic circumstances are interleaved with either a buffer or a register (n-bit) showing the possible variations on degradation of the signal integrity creating delays, attenuations of the amplitude or peak overshoots within the parameters.

The Analog signal is generated by Signal generator that is DAC block, The 3 - bit Flash ADC and 8-bit Sigma Delta ADC is generated using Vivado tool. Flash and Sigma-Delta (ΣΔ) ADCs work in tandem in a hybrid ADC design to balance resolution, speed, and power economy. The coarse quantization stage is handled by the Flash ADC, which uses an array of comparators to compare the input signal to several reference levels at once, providing incredibly fast conversion speeds. This makes the hybrid ADC perfect for high-frequency applications by allowing it to reach a high sampling rate. Flash ADCs, however, produce quantization errors and have a limited resolution. The residual signal from the Flash ADC is sent to the Sigma-Delta ADC for fine quantization in order to improve accuracy. To improve resolution and lower quantization noise, the ΣΔ ADC employs noise shaping and oversampling. The signal-to-noise ratio (SNR) and overall linearity are enhanced by its internal quantizer, which digitizes the filtered residue signal. The hybrid architecture can take use of both high-speed conversion and improved resolution thanks to the combination of Flash and ΣΔ ADCs. This architecture is commonly utilized in ultra-wideband applications, radar, and high-speed communication systems where high precision and quick sampling are crucial.

To improve accuracy, regulate time, or aid in quantization, a counter is frequently incorporated into the digital processing or calibration system of a hybrid ADC. Its main functions include monitoring the conversion steps, managing the stage sequencing, and supporting background calibration procedures. The counter can be utilized to synchronize the time between the Sigma-Delta (ΣΔ) ADC stages and the Flash ADC during the ADC operation. Counters in time-interleaved architectures control the channel switching by monitoring clock cycles, guaranteeing that various ADC channels sample the input signals at exact intervals. The counter functions as a binary code generator for the SAR logic in certain hybrid ADCs, particularly those that include successive approximation register (SAR) stages, regulating the bit-by-bit refinement of the digital output. It helps determine the final quantized value by iterating through the successive phases. Counters are also commonly employed in loops for background calibration. In this case, they measure timing discrepancies across channels or count the number of calibration cycles. The calibration system improves the overall linearity and accuracy of the ADC by lowering offset, gain, and timing errors through the counting and averaging of several conversion cycles. By monitoring the sampling points and coordinating the outputs from the coarse and fine quantization stages, counters in high-speed hybrid ADCs also aid in error correction and signal reconstruction. This guarantees that the Flash and ΣΔ ADC are properly combined to produce a high-resolution digital output in the end. All things considered, the counter in a hybrid ADC is essential for time management, synchronization, and calibration assistance all of which enhance the ADC's accuracy, linearity, and stability.

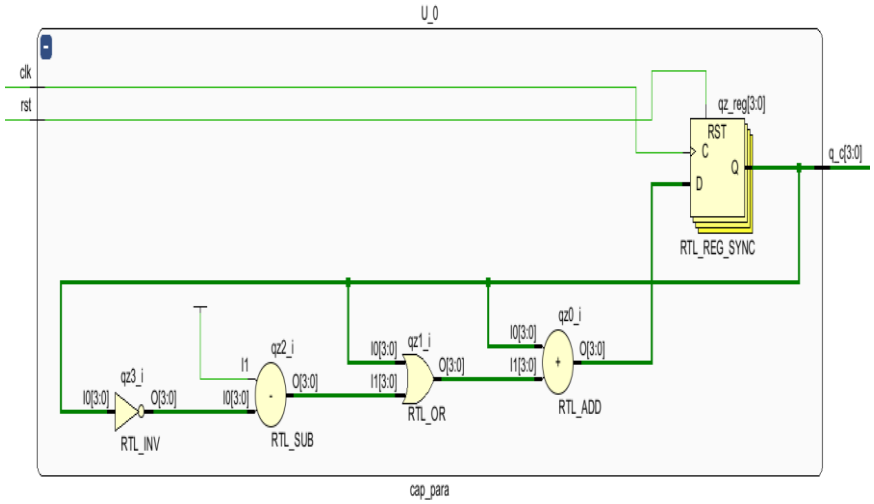

Figure.4.Represents the Internal RTL Schematic of Parasitic Capacitance

The Figure.4.Represents the Internal RTL Schematic of the parasitic capacitance of Hybrid ADC with Flash 3-bit and 8-bit Sigma Delta ADC design.

In hybrid ADCs, the counter-based linearity correction approach is a useful strategy for lowering non-linear errors brought on by timing skew, channel mismatches, and parasitic capacitance. Component mismatches, timing misalignment, and parasitic-induced distortions cause linearity errors in hybrid ADCs, which combine a Flash ADC for coarse quantization and a Sigma-Delta (ΣΔ) or SAR ADC for fine quantization. By

continuously monitoring the ADC's output over several conversion cycles, the counter approach resolves these problems. The counter tracks the difference between the output of the ADC and the anticipated linear response at each cycle. The system corrects offset, gain, and timing issues and lessens the effect of random noise by averaging the outputs over consecutive cycles. Because this dynamic correction procedure is carried out in the background, real-time calibration is ensured without interfering with the ADC's regular operations. By monitoring the sample order and implementing phase corrections, the counter in time-interleaved hybrid ADCs also plays a crucial part in synchronizing several channels, minimizing inter-channel mismatches and enhancing overall linearity. Consequently, the counter-based correction technique improves the ADC's signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR), making it ideal for high-speed applications including ultra-wideband radar, 5G communication, and high-resolution data acquisition systems. The Internal RTL Schematic of Shift Comparator in Hybrid ADC Design is Shown in below Figure.5

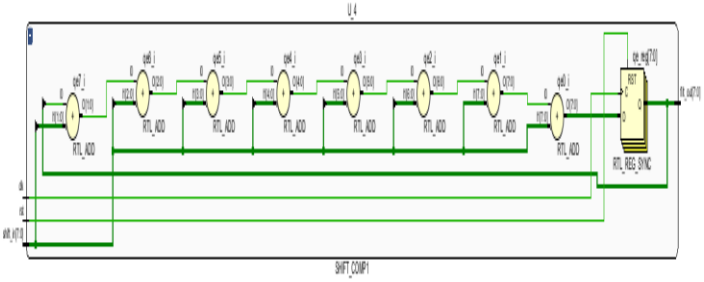

Figure.5. Represents RTL Schematic of Shift Comparator in Hybrid ADC Design

By lowering comparator offset and mismatch errors, the shift comparator technique is a useful way to improve linearity and accuracy in hybrid ADCs. Comparator mismatches cause non-linearities and offset errors that impair performance in hybrid ADCs, which usually combine a Flash ADC for coarse quantization and a Sigma-Delta (ΣΔ) or SAR ADC for fine quantization. In order to compensate for the discrepancies and enhance linearity, the shift comparator approach dynamically adjusts the comparator thresholds or the reference levels while they are operating. During the conversion process, this approach shifts the reference voltages or threshold levels applied to the comparators by a little, regulated amount. By ensuring that the comparator decision boundaries more evenly encompass the whole input range, this shifting procedure lessens the effect of comparator offset errors. By accounting for inter-channel mismatches, the shift comparator technique helps align the channels in time-interleaved hybrid ADCs, where multiple channels operate in parallel. This improves the overall signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). Furthermore, during several conversion cycles, the shifting procedure might be conducted in a random or cyclic fashion. The system efficiently eliminates offset and gain errors by averaging the outputs over a number of shifted cycles, enhancing the accuracy and linearity of the ADC. Because it allows dynamic calibration without the need for intricate external correction circuits, the shift comparator approach is especially advantageous for high-speed hybrid ADCs used in data acquisition, radar, and communication systems. For high-frequency applications, this makes the hybrid ADC more resilient and dependable by improving performance, decreasing non-linearity, and improving resolution.

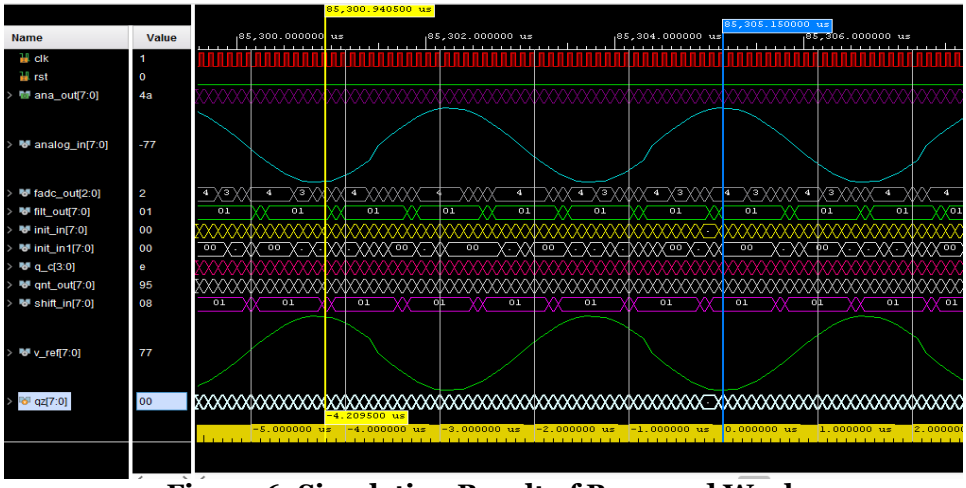

Figure.6. Simulation Result of Proposed Work

The above Figure.6. Shows the simulation result of Parasitic Capacitance using shift comparator with linearity error correction method .The Shift comparator signal is varied in accordance with the Analog input and V_ref signal. fadc_out is Flash ADC output and filt_out is Digital Filter which is followed by overall design to remove noise which is generating from Input signal.qnt_out is generated by the Sample - Hold Digital to Analog to Converter(SHDAC) to generate residual voltages which is from Flash ADC comparators.

Table.1 Shows Comparative Analysis of Proposed with other related works

Parameters	Proposed Work	[1]	[2]	[3]	[4]	[5]
Sampling Rate	**4.286 GSpS**	**1.6GSpS**	**3GSpS**	**2.5GSpS**	**2GSpS**	**4GSpS**
Resolution (bits)	**11**	**12**	**14**	**10**	**12**	**10**
SNDR	**68.98dB**	**40.79dB**	**75.5 dB**	**46.5dB**	**54.87dB**	**48.1dB**
Power	**0.0007 watts**	**11watts**	**98mw**	**10.5mw**	**895mw**	**9.4mw**
Effective Number Of Bits(ENOB)(bits)	**10.5**	**11.5**	**13.85**	**9.8**	**11.5**	**9.8**

Table.1. Comparison results of Proposed work

5. Future Scope

An innovative strategy that greatly improves performance, accuracy, and adaptability is the application of AI techniques in hybrid ADCs to manage parasitic capacitance. The impacts of parasitic capacitance, including non-linearity, offset errors, and gain fluctuations, intensify when hybrid ADCs run at higher sampling rates. It is frequently difficult for traditional correction methods to dynamically correct for these faults in real time. Artificial intelligence (AI) techniques, in particular machine learning (ML) algorithms, provide a potent remedy by continuously examining the output data from the ADC and spotting patterns brought on by parasitic-induced distortions. AI algorithms can minimize parasitic effects by adjusting internal parameters including comparator thresholds, reference voltages, and gain settings through real-time adaptive calibration. Furthermore, the linearity and spurious-free dynamic range (SFDR) of the ADC can be greatly enhanced using neural networks and reinforcement learning models, which can anticipate the non-linear behaviour brought on by parasitic capacitance and apply pre-emptive corrections.

AI can improve the overall signal-to-noise and distortion ratio (SNDR) in time-interleaved hybrid ADCs by identifying and fixing inter-channel mismatches brought on by parasitic fluctuations. Furthermore, by selecting applying correction only when necessary, AI techniques enable power-efficient calibration and lower the power overhead related to continuous calibration. More precision, speed, and power efficiency will be attained by hybrid ADCs as AI techniques advance, making them more appropriate for data collecting, radar, and next-generation 5G systems.

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