

Design and Analysis of Novel Inductor-Less Common Source Wideband CMOS LNA for IOT Applications

^{1*}Nishant Poras, ²Dr.Navaid Zafar Rizvi, ³Dr.Pradeep Tomar and ⁴Dr.Mangey Ram Nagar

^{1,3}Department of CSE, School of ICT, Gautam Buddha University, Greater Noida, India

²Department of Applied Sciences and Humanities, Jamia Millia Islamia, New Delhi, India

⁴Department of Electronics and Communication Engineering, Noida Institute of Engineering and Technology, Greater Noida, India

^{*}phdict2008@gbu.ac.in

ARTICLE INFO

ABSTRACT

Received: 29 Dec 2024

Revised: 15 Feb 2025

Accepted: 24 Feb 2025

The advent of technology has led to an exponential increase in data processing rates, particularly in wireless electronics networks. Low power consumption, low noise figure, and gain are key parameters in this context, especially for Internet of Things (IoT) devices. A low-noise amplifier (LNA) represents an essential RF component incorporated in almost every wireless network. Traditional LNA designs often rely on inductors, which can increase the size and power consumption of the device. Additionally, previous inductor-less LNA designs have struggled to achieve low noise figures and high gain simultaneously. This work addresses these challenges by presenting a novel inductor-less wideband common-source LNA, which achieves high gain and relatively low noise figure (NF) across a frequency range of 0.5 GHz to 2.6 GHz, which is required for wireless, portable, and Bluetooth devices. The design also incorporates a Balun in the test circuit of the proposed LNA to enhance signal integrity. Performance analysis displayed a Noise figure (NF) of 1.75dB, and S₂₂ is -17 dB, which shows that our output port is perfectly matched and delivers power efficiently to the load. In addition, the LNA demonstrates good input matching with S₁₁ of -10 dB and low reverse gain with S₁₂ of -20 dB, ensuring stable operation and minimal signal reflection. These metrics are excellent for inductorless LNA and a high gain (S₂₁) of around 23 dB compared to previous work. The proposed LNA was implemented using UMC 180nm CMOS process technology and simulated through Cadence Virtuoso Spectre RF. This research contributes to advancing wireless electronics networks by addressing the critical requirements of low power consumption and high performance, providing valuable insights for future LNA optimizations in IoT and other wireless applications.

Keywords: LNA, IoT, CMOS, common source, noise figure, S-parameters, RF.

I INTRODUCTION

LNA is the main component of the RF communication system, mainly located at the front end of the radio receiver circuit. It enhances faint signals by minimizing and mitigating the noise produced. As LNA is one of the active primary elements at the receiver end of the network, in RF communication, there is a considerable demand for LNAs that are small in size, which consume less power, provide sufficient gain, and have a very low noise figure. As IoT technology grows, less power consumption and less NF should be of more concern for IoT devices. The receiver is the component that should be optimized for smooth operation [1]

Wireless portable battery-powered devices, such as IoT devices, require more power, as most IoT devices are battery-operated, resulting in high power consumption. High noise is primarily present in all RF front-end circuits, like LNA and mixer, due to continuous movement [2], so there is a necessity for the design of RF circuits that consume less power, have a low die area, and offer good gain and improved noise figure. As the semiconductor industry is approaching towards lower technology nodes lower nodes in CMOS technology can be used for low power design and making device compact but in this main challenge is that if existing circuit topology used then it comes with some drawbacks such as velocity saturation, degradation in mobility, output conductance and its transit frequency [3-4]. Inductor-less LNA is most suitable for RF circuits required for IoT applications [5] because inductor-less LNAs consume less area on the chip and losses are reduced, so power consumption is low, and the performance metrics of LNAs are improved.

Inductorless shunt feedback LNA is proposed in [6]. In this work, feedback between the output and the input results in impedance matching.

Current efficiency also improves because of the feedback current used by the main transistor. In this LNA, power consumption is very low because of low transconductance, and it occupies less area on the chip (0.0052 mm²), but the noise figure deteriorates in this work. As the frequency increases, the performance of LNAs can encounter various challenges. Multi-standard LNAs present several advantages such as reduced die area, lower power consumption, wideband capability, and improved system matching. Given the growing demand for multi-standard devices, the trend in LNA design seems to be shifting from single-standard to multi-standard LNAs, with distinct methodologies and topologies evident in existing literature [7]. LNA low-power topologies have been described in the literature [9-16]. Low-power LNAs are designed using methods that incorporate current reuse coupled with negative feedback [9], inductive degeneration [10], active shunt feedback [6], and forward bias (FBB) [12]. Shunt feedback with double capacitance cross-coupler [13].

After studying the low-power LNA topologies of previous work, feedback techniques were found to be more suitable for low-power design and low-power (sub-mW) models [9,6, 12, 14, 16]. It is difficult to achieve a noise figure (NF) less than 3 dB [13]. However, achieving this low noise figure comes at the expense of sacrificing linearity [15]. Extra transistors were incorporated in the circuit to overcome this issue, which may cause poor process and mismatch [15]. Therefore, LNA should be designed with techniques that help achieve less than 3 dB NF in operation [1]. This work proposes an efficient low-power wideband CMOS LNA for front-end applications. It is particularly suitable for IoT applications because its design does not use inductors and has fewer transistors, reducing power consumption and noise figure. Additionally, the gain of the LNA is increased. Furthermore, the proposed LNA is less complex and requires less chip area, making it ideal for IoT applications operating at low voltage. The proposed LNA is implemented in Cadence Spectre 180nm CMOS technology.

This paper is partitioned into various sections. The introduction is in section I above. The topology of our proposed LNA with mathematical expressions of parameters is described in Section II. The design and simulation of the proposed LNA are defined in Section III. Results of our work are described in Section IV, and the conclusion of this work is described in Section V.

II TOPOLOGY OF PROPOSED LNA

This work employs the design of the LNA without using bulky component inductors to achieve a low-noise figure. If the noise figure of the first stage of the LNA network is reduced, then the noise figure of the entire RF circuit is decreased. The Friis equation can also validate this.

$$F_{TOT} = F_1 + \frac{F_2-1}{A_1^2} + \frac{F_3-1}{A_1^2.A_2^2} \quad (1)$$

According to the equation above, it is essential in our design to have a minimum Noise Figure for the first stage as much as possible. The common-source LNA with biasing at the ideal operating point is proposed in this work because CS LNAs have good gain and low noise figures. It is obtained because of the biasing of a transistor for small signal operation. The proposed common-source LNA offers good impedance as matching is done for both input and output. It is suitable for IoT devices as our LNA design is inductorless, and resistors and capacitors are used for impedance matching. Matching is done in a way that ensures maximum power transfer over a wide frequency range, making the proposed LNA suitable for wideband operations. First, MOSFETs at the input stage and MOSFETs at the output stage act as the core of the LNA, and they behave as amplifying elements. MOSFETs used in this proposed design have low threshold voltage and gate leakage to reduce the power consumed by the circuit. In this design, the output stage is a source follower, which drives the next stage, typically a mixer or other test equipment. The designed LNA is a multi-standard cascode common-source (CS) LNA.

S-Parameter analysis

S-parameters (scattering parameters) are used to identify the performance of LNA based on how signals are passed throughout the device through the device by calculating the S-parameter of LNA we can find about gain, noise, matching (both input and output) and stability of LNA, the main advantage of the s parameters is that they can be

measured by impedance matching i.e. by taking a reference impedance the source and load impedances are matched. S-parameter of two-port networks, such as LNA, is shown in Fig. 1. So, Fig. 1 shows that the normalized incident wave a_1 is entering the network at port i, as well as its reflected voltage wave b_1 leaving port i, which is measured. The equations below give these normalized incidents and reflected waves (a_1 and b_1) related to the terminal voltage and currents at port i.

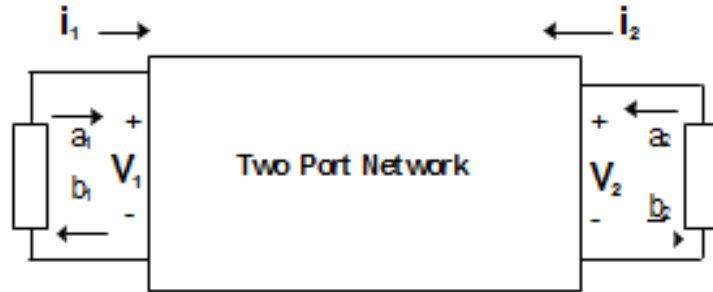


Fig.1. Two Port

$$a_i = \frac{v_i + Z_{0i}}{2\sqrt{Z_0}} \quad (2)$$

$$b_i = \frac{v_i - Z_{0i}}{2\sqrt{Z_0}} \quad (3)$$

Where reference impedance is represented by Z_0 (in this analysis, it is assumed to be real, whereas usually it is equal to 50 Ω), the contributions from the two ports can be combined to form equation 4(matrix) for the network.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (4)$$

In the above equation, S_{11} , S_{12} , S_{21} , and S_{22} are the s-parameters, i.e., scattering parameters measured across the ports 1 and 2 of the two-port network, in which S_{11} and S_{22} are reflection coefficients, whereas S_{12} and S_{21} are transmission coefficients of LNA. S_{11} assesses input matching and impedance mismatch losses, and S_{22} is used for output matching losses. S_{21} is an essential parameter of LNA used for the calculation of gain, and S_{12} is for the stability of LNA. We can evaluate the performance of our proposed LNA.

Gain Analysis

The ratio of the reflected wave (voltage wave) leaving the port to the incident wave(voltage) entering the port is known as the reflection coefficient, and it is expressed by the equation 5 given below.

$$\left[\Gamma = \frac{Z - Z_0}{Z + Z_0} \right] \quad (5)$$

Power gains of two-port networks are given below by equations 6, 7, and 8.

$$G_T = \frac{P_L}{P_{AVS}} \quad (6)$$

$$G_P = \frac{P_L}{P_{IN}} \quad (7)$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} \quad (8)$$

G_T is referred to as the power gain of the transducer. The power gain of a transducer indicates the power delivered at the load, i.e., load mismatch, which relates to the power available from the source, i.e., source mismatch. G_P is power gain, which signifies the power supplied to the load if a load mismatch originates from the power input into the network. Conversely, G_A refers to the power gain available in the network. It illustrates the power accessible from the network under matched load conditions and concerns the power available from the source with source

mismatch. It's important to note that the transducer gain (G_T) will always be less than or equal to G_A and G_P . However, when source and load are matched to the output and input impedance of the two-port network, all power gains become equal. So, by this, we can evaluate the efficiency of RF and microwave systems, concerning power transfer and impedance matching.

$$G_T = \frac{1-|\Gamma_S|^2}{1-|\Gamma_N S_{21}|^2} |S_{21}|^2 \frac{1-|\Gamma_L|^2}{1-|S_{22}\Gamma_L|^2} \quad (9)$$

$$G_T = \frac{1-|r_s|^2}{1-S_{11}|r_s|^2} S_{21} \frac{1-|r_l|^2}{1-T_{out,r}|r_l|^2} \quad (10)$$

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2} |S_{21}|^2 \frac{1-|\Gamma_L|^2}{1-|S_{22}\Gamma_L|^2} \quad (11)$$

$$G_A = \frac{1-|\Gamma_{IN}|^2}{1-S_{11}|\Gamma_{IN}|^2} |S_{21}|^2 \frac{1}{1-|\Gamma_{OUT}\Gamma_L|^2} \quad (12)$$

Reflection coefficients are written in equation 9. The alternate expressions for Γ_{IN} and Γ_{OUT} given in equations 13 and 14, if input and output impedances (Z_{in}, Z_{out}) are unknown

$$\Gamma_{IN} = \frac{S_{11}+S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad (13)$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \quad (14)$$

Voltage gain is defined as:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (15)$$

By using the above equations, an expression for the voltage gain deducted is as follows: -

$$A_v = \frac{S_{21}(1+\Gamma_S)}{(1-S_{22}\Gamma_L)+S_{11}(1-S_{22}\Gamma_L)+S_{12}S_{21}\Gamma_S\Gamma_L} \quad (16)$$

Noise Analysis To find the noise figure, the noise factor of LNA should be analyzed [8]

$$F = \frac{SNR_{IN}}{SNR_{OUT}} = \frac{P_{noise,output}}{GP P_{noise,source}} \quad (17)$$

Where GP is the power gain, the Noise factor at the input

$$F = \frac{i_s^2 + |i_n + Y_s v_n|^2}{i_s^2} \quad (18)$$

Where is

$$i_n = i_c + i_n \quad (19)$$

$$Y_c = \frac{i_c}{v_n} \quad (20)$$

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f} \quad (21)$$

$$G_u = \frac{\overline{i_u^2}}{4kT\Delta f} \quad (22)$$

$$R_s = \frac{\overline{i_s^2}}{4kT\Delta f} \quad (23)$$

By the above equations, the noise factor can be:

$$F = 1 + \frac{G_u + |Y_c + Y_s| \sqrt{R_n}}{G_s} \quad (24)$$

The amount of noise injected into the circuit is known as the noise figure (NF). As the noise factor is calculated above, the Noise figure expressed in decibels is written as

Noise figure (dB) = $10 \log_{10} (F)$ (25)

III DESIGN OF PROPOSED LNA

The LNA proposed in this work uses Cadence Spectre 180nm CMOS technology. This paper includes a new idea for designing an LNA that consumes less power and reduces the noise figure compared to the previously done work. In this work, LNA is designed without an inductor because an inductor is a bulky component that increases losses and chip area, and, in this work, a less complex architecture of Multiband LNA is used in which the number of transistors is reduced and with a single source of voltage supply. Biasing of the transistors is done at an ideal operating point, which minimizes the noise. At the same time, its gain remains unaffected, and impedance matching also reduces the circuit's noise figure (NF). The proposed LNA operates on a frequency range from 0.5 GHz to 2.9 GHz, i.e., it covers almost all the IoT and other data applications such as UMTS, GSM, Bluetooth, and Wi-Fi applications. It is a multi-standard Cascode Common Source LNA (CS-LNA). The LNA is designed using a CMOS 180nm technology process with a 1.3V power supply. The advantage of our proposed LNA is a smaller package size, less cost, Large-scale integration, less complexity, a low noise factor, power, Wider operating temperature, lower operating voltage, and Low power consumption because it does not have an inductor, which consumes more, making it suitable for IoT applications.

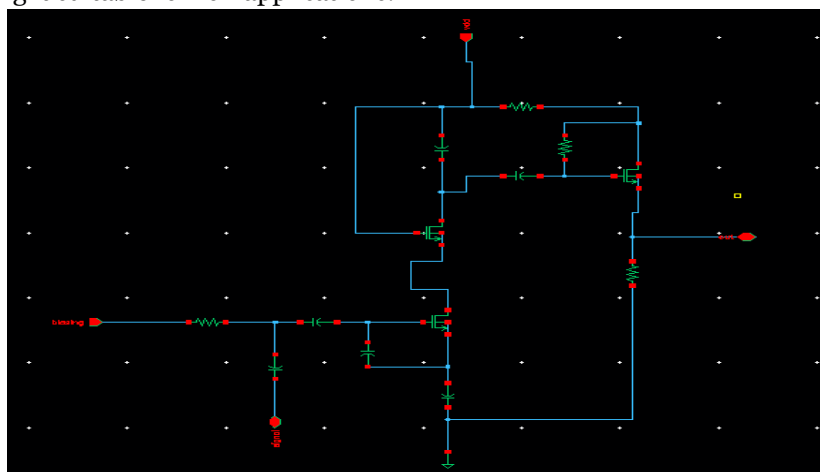


Fig. 2. Schematic of LNA

This schematic represents a compact, inductor-less, low-noise amplifier designed for wideband operation. Instead of using bulky inductors, the design relies on a combination of resistors, capacitors, and active transistor stages to achieve signal amplification. At its core, a common-source transistor amplifies the input RF signal, while additional stages, such as cascode and source follower configurations, enhance gain and improve isolation. The circuit also includes matching networks that ensure proper impedance at both the input and output, which is crucial for minimizing signal reflection. This design prioritizes low power consumption and a reduced chip area, making it well-suited for IoT and portable wireless applications.

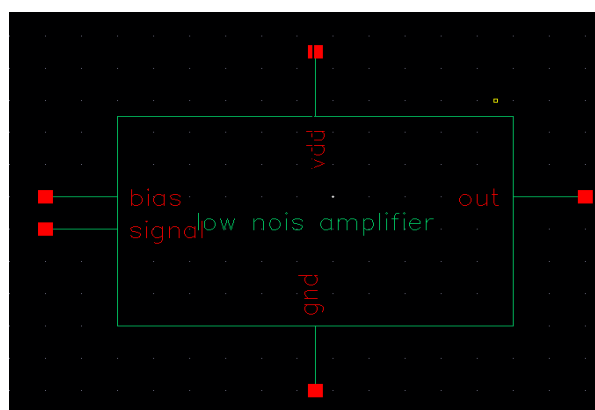


Fig. 3. Symbol of LNA

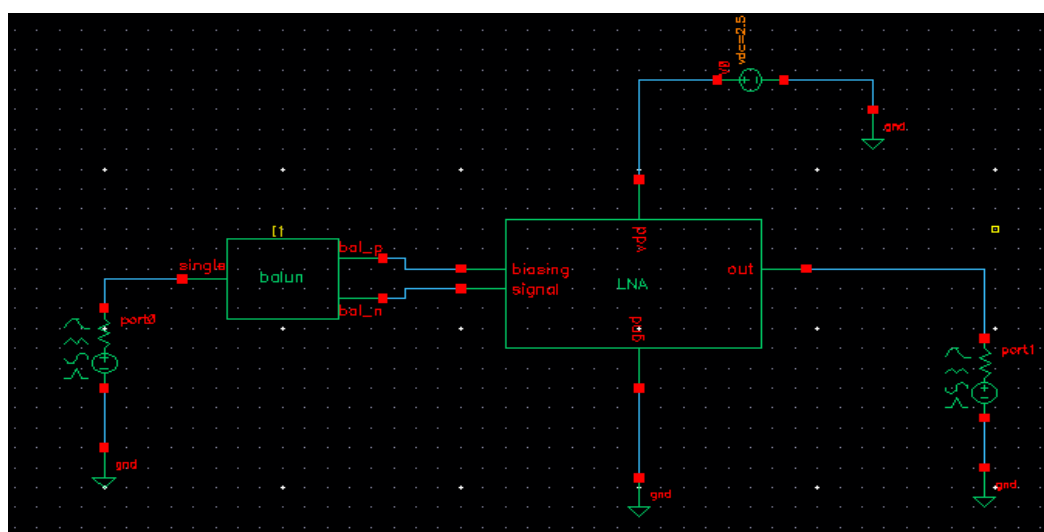


Fig. 4. Test circuit of LNA

TABLE 1: INVENTORY OF TEST CIRCUIT

Sr.No.	COMPONENTS USED	NOS
A	RESISTOR	4
B	BALUN	1
C	CAPACITOR	6
D	NODES	12
E	BSIM3V3	3
F	PORT	2
G	VOLTAGE SOURCE	1

After designing the schematic in Cadence as shown in Fig. 2, we generate the symbol of the LNA for running a simulation and to get the desired result efficiently, the symbol designed in Cadence is shown below in Fig. 3. After generation of symbol of LNA then a test circuit is designed and simulations is done for different parameter. LNA test circuit is shown in Fig. 4. LNA is shown as a two-port network, which has two ports (port 0 & port 1) as input and output ports with output matching and biasing as shown in the test circuit Fig. 4. Balun is used in our LNA test circuit. A balun is used here to combine a balanced line with an unbalanced line. It matches different types of transmission lines as per the it is just like a type of transformer that converts associate degree unbalanced signal into a balanced signal and it also isolates transmission line and supplies a balanced output which improves the performance of the circuit as it also helps in matching the impedance of the circuit so signal distortion is minimized.

BSIM3 is a MOSFET SPICE model used in designing and simulating semiconductor circuits and developing CMOS technology. Bsim3v3 is a sub-micron MOSFET model used in the optimization and development of integrated circuits, and it also predicts the performance of electronic circuits. Setup of test circuit of proposed LNA as a two-port, i.e., input and output ports, as shown in Fig. 5. The Input port is named port 0 in the test circuit, and the output port is named port 1. The source of the Input port is a sine wave with a resistance of 55 ohms, and the Output Port in the LNA test circuit has a resistance of 500 ohms, and the port number is given as 1. Component values in the test circuit, i.e., the DC source Vdc, are 2.5V. This novel schematic does not have inductors like traditional narrowband LNAs with large spiral inductors for matching or load. The load and matching are performed by resistors, capacitors, and transistor configurations, i.e., cascode/source follower, making the design more compact and suitable for multi-band or wideband applications.

IV. RESULTS AND DISCUSSIONS

The Cadence IC Virtuoso tool obtains the proposed LNA's performance analysis and simulation results. The CMOS 180nm technology process is used for this. The noise contribution and gain exhibited by the LNA are calculated using S-parameter analysis. S_{11} and the output matching by S_{22} analyze the input matching.

After the simulation, it was observed that the LNA provides suitable input matching, as the results showed a negative value of S_{11} . The result obtained by s-parameters simulation and analysis for S_{11} , S_{22} , S_{12} , shows improvement in performance and viability for RF wireless communication because the result obtained from the simulation of S_{11} , S_{22} , S_{12} are below zero i.e, there values are negative and because of this good amplification factor is provided to the circuit and as S_{11} and S_{22} both are negative. This indicates satisfactory input and output matching because ideally, S_{22} and S_{11} are zero, which means the ports are perfectly matched. Forward gain is obtained by parameter S_{21} . Reverse voltage gain is obtained by simulation of S_{12} . The output voltage reflection coefficient is obtained by S_{22} analysis, and the S_{11} curve is plotted to get the input voltage reflection coefficient values. So, after obtaining values of S-parameters with simulation values, an enhanced performance of the proposed LNA is shown. An S-parameter analysis of our proposed LNA shows that this LNA has a more optimized performance than the previously designed LNA using bulky inductors.

As S_{11} and S_{22} are negative, it is enough to indicate a satisfactory input matching and output matching because ideally, S_{11} and S_{22} are zero, meaning that ports are perfectly matched. S_{12} of the proposed LNA is shown in Fig. 5, around -20dB, which indicates that the proposed LNA has good reverse gain, preventing unwanted signals from coupling to the input. Parameter S_{22} of LNA is shown in Fig. 6. S_{22} shows the reverse isolation, around -17 dB, so our LNA is feasible as the value of S_{22} is negative, and the LNA reasonably matches its input. The reverse transmission parameter, S_{12} , which measures the isolation between the output and input ports, is also negative, as shown in Figure 5. This indicates strong reverse isolation, effectively preventing unwanted signals from coupling back to the input, which could otherwise lead to feedback-induced instability or performance degradation. The proposed design significantly reduces the chip area by eliminating inductors, a critical consideration for compact devices like IoT sensors and wearable electronics. This reduction also lowers manufacturing costs and challenges associated with inductor quality factors, parasitic effects, and process variations, which can degrade performance in inductor-based LNAs. Despite the absence of inductors, the proposed LNA achieves exceptional performance metrics, demonstrating that innovative circuit techniques can compensate for the lack of inductive elements, making it a cost-effective and scalable solution for mass production.

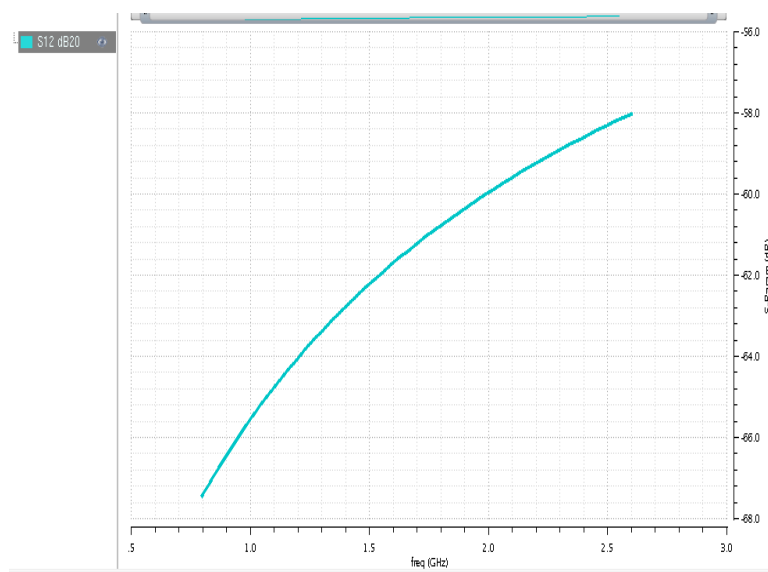
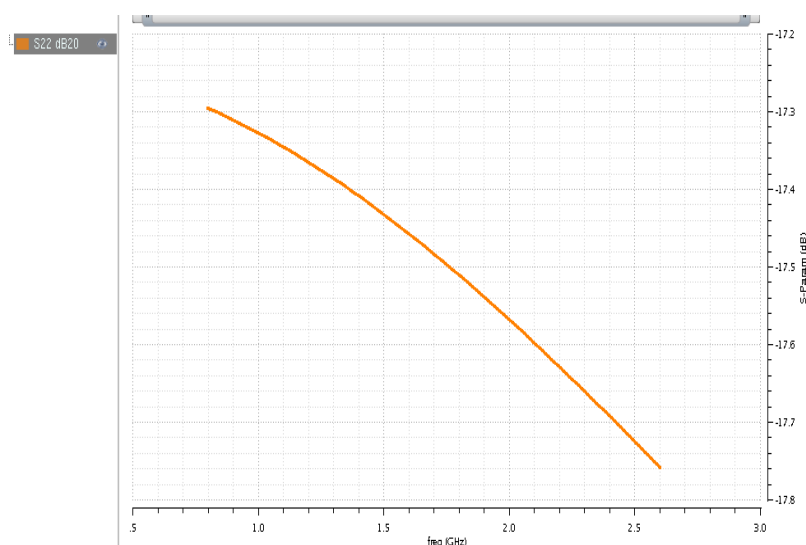
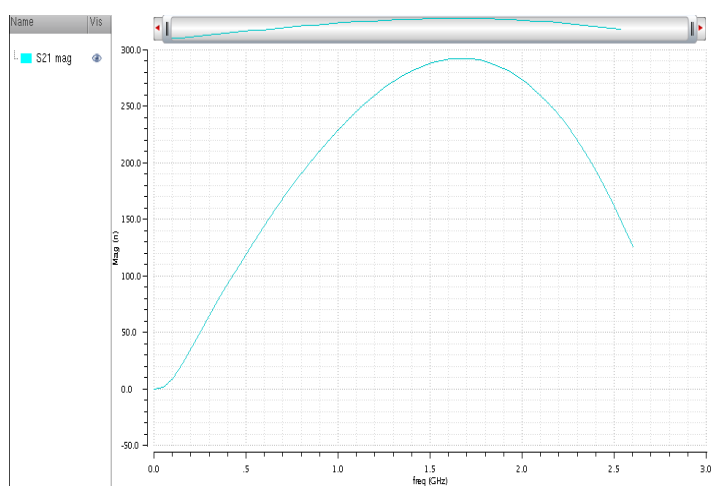


Fig. 5. S_{12} of LNA

Fig. 6. S₂₂ of LNA

S₂₁ in mag is shown below in Fig.7. S₂₁ is the forward gain of LNA if S₂₁ is the greater S₂₁ magnitude of LNA. The higher the magnitude, the higher the amplification given by the LNA. The S₂₁ is around 23dB when converted from mag to dB. Highlighting the LNA's capability to provide efficient signal amplification. This high gain is particularly significant in the absence of inductors, achieving such amplification levels in the absence of inductive components traditionally used for impedance tuning and gain enhancement. Fig.8 shows S₁₁ of LNA, i.e., the Forward reflection coefficient is negative around -1.7 dB, which shows that the proposed LNA has a reasonable match to its input and that the LNA has good impedance matching. The negative values of S₁₁ and S₂₂ achieved here are sufficiently low to confirm satisfactory matching, which is most important in optimizing the LNA's performance in practical RF systems.

Figure 9 below shows the Noise figure (NF) of our proposed LNA. The NF is around 1.75 dB, which shows significant results compared to the previous work. It improves the system sensitivity of our LNA. So, because of the low NF, the signal-to-noise ratio of our LNA will be high, and the FOM of the LNA will be good. This low NF is a standout feature, as it outperforms many previous designs, including those cited in recent literature, enhancing the LNA's sensitivity to weak signals. A lower NF translates to a higher signal-to-noise ratio (SNR), vital for applications like Internet of Things (IoT), Wi-Fi, and Bluetooth, where detecting and amplifying low-power signals with minimal distortion is paramount. Compared to prior work, such as reference [1] with an NF of 1.72 dB but a lower gain of 18.9 dB, this design achieves a superior noise performance and amplification balance, showing its efficacy for high-sensitivity applications.

Fig. 7. S₂₁ of LNA

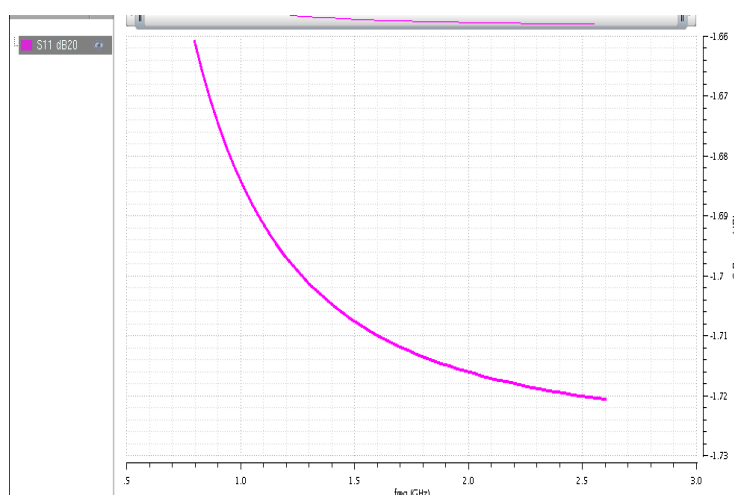
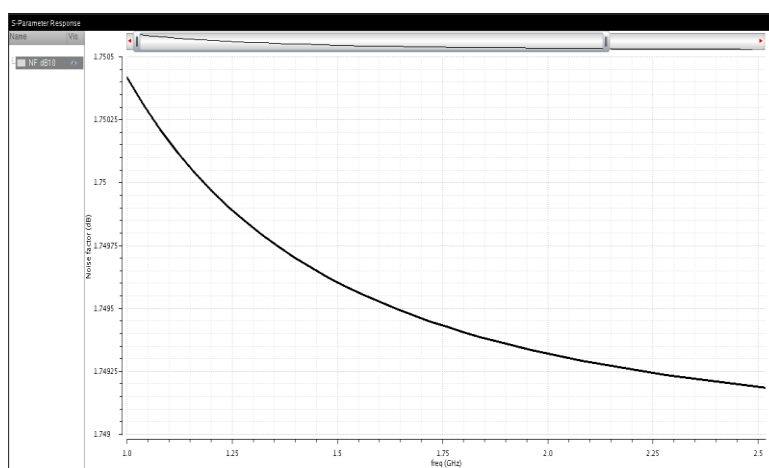
Fig. 8. S_{11} of LNA

Fig. 9. Noise Figure of Proposed LNA

The LNA's ability to operate across a wide frequency range of 0.5 to 2.6 GHz further enhances its versatility, enabling multi-standard functionality. This broad bandwidth allows the amplifier to support multiple wireless communication protocols, such as Wi-Fi, Bluetooth, and cellular bands, within a single design, eliminating the need for various LNAs tailored to specific standards. This feature is increasingly valuable in modern wireless systems, where devices must seamlessly handle diverse frequency bands and protocols. For instance, IoT devices often require compatibility with various networks, and this LNA's wideband operation simplifies system integration while reducing power consumption and cost compared to deploying multiple narrowband amplifiers.

Table 2 Comparative Analysis of results with existing state-of-the-art

Design	Frequency range	Multi-standard	NF	Gain	Published Year
This work	0.5-2.6 GHz	Yes	1.75 dB	23dB	To be Published
[17]	0.1–3.1 GHz	No	4 dB	18 dB	2024
[18]	2.5 GHz	No	2.5 dB	18.87 dB	2021
[19]	26GHz-32GHz	No	2.6 dB	16.9 dB	2024
[1]	100 MHz to 3.27 GHz	No	1.72 dB	18.9 dB	2024
[20]	3.2-9.62 GHz	No	4.5 dB	9.94 dB	2021

This novel work delivers the highest gain and lowest noise figure, which is most important for IoT, Wi-Fi, and other Bluetooth wireless applications. The proposed work provides the best signal amplification and sensitivity in the desired frequency band compared to the previous work. [21] shows a good noise figure, but it is designed using a MIM capacitor, unlike this work, which is designed without an inductor. Table 2 above shows the comparison of our novel design with the latest published works, as evident from the comparative analysis that this design offers the best noise figure and gain, even in the absence of an inductor, and with its multi-standard design, it can work at different frequency bands simultaneously.

V CONCLUSION

This research introduces a novel wideband low-noise amplifier (LNA) designed and simulated using the Cadence Virtuoso tool within a 180nm CMOS technology node. The proposed inductor-less LNA demonstrates significant advancements in critical performance metrics, making it an ideal candidate for modern wireless communication systems, particularly Internet of Things (IoT) applications. Key achievements include a noise figure (NF) of approximately 1.75 dB and an exceptional gain (S_{21}) of 23 dB across a frequency range of 0.5 to 2.6 GHz. These specifications ensure high sensitivity and robust signal amplification, catering to multi-standard wireless technologies such as Bluetooth, Wi-Fi, UMTS, and GSM.

The design's inductorless architecture eliminates the need for bulky inductors traditionally used for impedance matching and load purposes, replacing them with resistors, capacitors, and optimized transistor configurations (e.g., cascode and source follower stages). This approach reduces power consumption and minimizes chip area, addressing the pressing demands for compact, energy-efficient RF circuits in portable and battery-operated devices. The LNA achieves excellent output matching, as evidenced by an S_{22} parameter of -17 dB, which indicates minimal signal reflection and efficient power delivery to the load. Additionally, the input matching (S_{11}) and reverse isolation (S_{12}) parameters further confirm the design's stability and performance, ensuring satisfactory impedance matching and reduced signal coupling back to the input.

A comparative analysis with state-of-the-art LNA designs highlights the superiority of this work. Unlike previous designs that often rely on inductors and achieve noise figures above 2.5 dB or gains below 20 dB, this LNA outperforms them with a lower NF and higher gain, even without inductors, while maintaining wideband capability. Using fewer transistors and a single 1.3V supply voltage enhances its simplicity and cost-effectiveness, making it a practical solution for large-scale IoT and other wireless systems integration. The inductor in the test circuit further improves signal integrity, reducing distortion and enhancing impedance matching across the wide frequency band.

This research delivers a high-performance, area-efficient, and power-efficient LNA that sets a new benchmark for inductor-less designs. Achieving an optimal balance of low noise, high gain, and wideband operation provides a valuable contribution to the advancement of RF front-end circuits. This work meets the current demands of IoT and wireless communication systems and lays a strong foundation for future innovations in low-power, high-performance RF electronics. This LNA design makes the way for several exciting research and development opportunities, as this design can be implemented in lower advanced CMOS nodes (e.g., 90nm, 65nm, or below), which could further reduce power consumption and chip area while potentially enhancing performance metrics such as gain and noise figure. This would align with the semiconductor industry's miniaturization and circuit efficiency trend. Future work could improve the LNA's capability to process variations, temperature fluctuations, and voltage supply changes, ensuring consistent performance in different operating conditions. So this research could be helpful in next-generation RF circuit design, driving innovations that meet the growing demands of IoT, wireless connectivity, and beyond.

ACKNOWLEDGMENT

Authors express gratitude to the entire faculty and the Lab in charge of the School of Information and Communication Technology at GBU, Greater Noida, for their invaluable guidance and provision of necessary resources for this work, and special gratitude to my research supervisors for providing me with their valuable time and guidance needed to complete this work.

REFERENCES

- [1] R. Zhou, J. Yang, L. Wang, X. Zhao, S. Liu, and D. Sun, "A wideband low power RF Receiver Front-End for Internet-of-Things applications," *Microelectronics Journal*, vol. 144, 2024, Art. no. 106064.
- [2] S. C. Gladson and M. Bhaskar, "A low power high-performance area efficient RF front-end exploiting body effect for 24GHz IEEE 802.15.4 Applications," *AEU International Journal of Electronics and Communications*, vol. 96, pp. 81–92, 2018.
- [3] A. Balankutty and P. R. Kinget, "An ultra-low voltage, low-noise, high linearity 900-MHz receiver with digitally calibrated in-band feed-forward interferer cancellation in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2268–2283, 2011.
- [4] S. Shameli, A. Amin, and P. Heydari, "A novel power optimization technique for ultra-low power RFICs," in *Proceedings of the 2006 International Symposium on Low Power Electronics and Design*, Oct., pp. 1–4, 2006.
- [5] M. Gupta and M. Kumar, "Low Power Inductorless LNA using Noise Cancellation Technique for UWB Applications," in **J. Phys.: Conf. Ser.**, vol. 1947, article 012027, 2021.
- [6] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback," **IEEE Transactions on Microwave Theory and Techniques**, vol. 64, no. 6, pp. 1843–1853, Jun. 2016.
- [7] M. B. Thacker, M. Awakhare, R. H. Khobragade, and P. A. Dwaramwar, "Multi-Standard Highly Linear CMOS LNA," in **Proceedings – IEEE International Conference on Electronic Systems, Signal Processing, and Computing Technologies, ICESC 2014**, pp. 63–68, 2014.
- [8] A. Van Der Ziel, "Noise in Solid State Devices and Circuits", Wiley, New York, 1996.
- [9] M. Parvizi, K. Allidina, F. Nabki, and M. El-Gamal, "A 0.4V ultra low-power UWB CMOS LNA employing noise cancellation," in *IEEE International Symposium on Circuits and Systems*, 2013.
- [10] Z. Li, L. Sun, and L. Huang, "0.4 mW wideband LNA with double gm enhancement and feed-forward noise cancellation," *Electron Lett*, vol. 50, no. 5, pp. 400–401, 2014.
- [11] M. Parvizi, K. Allidina, and M.N. El-Gamal, "A sub-mW, ultra-low-voltage, wideband low-noise amplifier design technique," *IEEE Trans. Very Large Scale Integration. VLSI Syst.*, vol. 23, no. 6, pp. 1111–1122, 2015.
- [12] S. Pandey and J. Singh, "A low power and high gain CMOS LNA for UWB applications in 90nm CMOS process," *Microelectron J*, vol. 46, pp. 390–397, 2015.
- [13] M. Parvizi, K. Allidina, and M.N. El-Gamal, "Short channel output conductance enhancement through forward body biasing to realize a 0.5 V 250 μ W 0.6–4.2 GHz current-reuse CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 574–586, 2015.
- [14] R. Jafarnejad, A. Jannesari, A. Nabavi, and A. Sahafi, "A low power low noise amplifier employing negative feedback and current reuse techniques," *Microelectron J*, vol. 49, pp. 49–56, 2016.
- [15] A. Khabbaz, J. Sobhi, and Z.D. Koozehkanani, "A sub-mW 2.9-dB noise figure Inductor-less low noise amplifier for wireless sensor network applications," *AEU Int. J. Electron. Commun.*, vol. 93, pp. 132–139, 2018.
- [16] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband inductorless low-power LNAs with Gm enhancement and noise-cancellation," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 1, pp. 26–38, 2018.
- [17] Singh V, Kumar M, Kumar N (2024) Design of a low-power LNA circuit with noise canceling approach in 90 nm CMOS process. *Integration* 96:102163. <https://doi.org/10.1016/j.vlsi.2024.102163>.
- [18] Gladson SC, Harikumar R (2021) A 219- μ W ultra-low power low-noise amplifier for IEEE 802.15.4 based battery-powered, portable, wearable IoT applications. *Discover Appl Sci* 3(4):1–12.
- [19] Kalra D, Srivastava M, Design and optimization of variable gain LNA for IoT applications using meta-heuristics search algorithms *MicroelectronEng* 286:112125., 2024 <https://doi.org/10.1016/j.mee.2023.112125>
- [20] Tarighat, A.P. Ultra-low power inductorless differential LNA for WSN application. *Analog Integr Circ Sig Process* **108**, 409–419 (2021). <https://doi.org/10.1007/s10470-021-01892-1>.
- [21] Nishant Poras, Priyanka Goyal. Design and Performance Analysis of Multi-Standard CMOS LNA Using Switched Capacitor and MIM Capacitor in 180 nm Technology. *Journal of VLSI Design Tools and Technology*. 2015; 5(3): 37–44p.