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Ensuring Low-Power Design Verification in Semiconductor Architectures

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ABSTRACT

With rising energy demands on both sides of the memory and compute stack in high-performance computing (HPC), graphics, and artificial intelligence (AI) accelerators, high energy efficiency, low latency, and scalable semiconductor designs have become important. As these industries develop, well-thought-out conservation in the semiconductor architecture is necessary to pursue economic and environmental goals. This paper studies the role of low-power design verification in semiconductor architectures in terms of some key methodologies, such as Design for Test (DFT) and GPU hardware validation, respectively. The verification process verifies the performance, power, and functional requirements compulsory in low-power applications. It shows how powerful the DVFS, clock, and power gating techniques reduce power consumption. The scan chain insertion, built-in self-test (BIST), and boundary scan are required DFT methodologies to help identify early in the design cycle and before full design. These power inefficiencies would otherwise require a costly redesign once a portion of the design is available in production. Finally, the paper also talks about the role of GPU hardware validation in guaranteeing that AI accelerators work effectively with power limitations. The paper points out that following the integration of power-aware simulation tools and cooperation among multidisciplinary teams, low-power design verification can be useful in designing energy-efficient, high-performance semiconductor devices. The last study looks at future design verification of low-power technology, which will continue to enable energy-efficient semiconductor technology by integrating AI-driven tools and quantum computing. A contribution to understanding how verification is fundamental to realizing sustainable and optimized design for future semiconductors is made.

Keywords: Low-power design verification, Semiconductor architecture, Design for Test (DFT), GPU hardware validation, Dynamic voltage and frequency scaling (DVFS), First-time-right silicon

1. Introduction

Over the past few years, energy-efficient semiconductor designs have become the order of demand due to the ever-unceasing development process in high-performance computing, graphics, and artificial intelligence (AI) accelerators. With industries increasingly relying on these technologies, reducing power to semiconductor architecture has become more critical than ever before. It is about providing this performance and finding a balance of power consumption that meets strict energy efficiency requirements. In particular, given the importance of power efficiency in applications such as mobile devices, data centers, and AI-powered systems, which are also crucial from economic and environmental perspectives, making energy-efficient data structures is especially important. These advanced technologies are developed based on low-power design in the semiconductor architecture. For instance, high-performance computing and AI accelerators must rapidly apply complex computations while consuming little energy. GPUs are used quite widely today in gaming and obviously in AI and machine learning, and it is necessary to have efficient power management so that GPUs can perform at the level they need to without too much energy consumption. These designs require the power features to be integrated to reach performance and environmental standards. Nevertheless, due to the rigorous validation processes that are essential throughout the development lifecycle, ensuring a design is both functional and energy efficient from the onset is complex.

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Achieving power-efficient semiconductor designs requires an integral role in design verification. Here, functional correctness, as well as performance optimization, is confirmed by this process through different conditions. As verification is directly relevant to power consumption, it is even more important in low-power designs. The engineer can uncover potential cases by using advanced verification techniques, circumventing additional redesign or performance bottlenecks. The design must be verified to meet power constraints during simulation or physical testing to ensure that the semiconductor runs efficiently in the real world. Thorough verification of the universality constraint is critical since doing so will minimize the risk of energy inefficiency that can result in performance degradation, overheating, and so on, which can diminish the system's reliability. A couple of critical technologies and methodologies are embedded in low-power design verification. Design for Test is one methodology where testability is designed into the design process to be functional and efficient for power management features. After that, DFT allows for the insertion of specific test structures (scan chains) to be able to probe in detailed power consumption analysis during the testing phase. This is a critical capability for finding power inefficiencies in the design before completion. Furthermore, GPU hardware validation is essential during the graphics processing unit and AI accelerator power reduction as part of the low-power verification process. GPU validation ensures these high-performance units work correctly by validating power consumption on multiple workloads, finding places to optimize, and ensuring that power management systems behave as expected while loaded.

This work aims to understand the importance of low-power design verification concerning semiconductor architectures and their technology, such as Design for Test (DFT) and GPU hardware validation. This paper aims to give a complete picture of how these verification techniques contribute to building power-efficient semiconductor designs. This study will glean from current best practices, successful case studies, and maybe even future trends in this new realm of low-power semiconductor design to draw implications on the future of low-power semiconductor design and its subsequent importance in driving advancements of high-performance computing, graphics, and AI technologies. The paper introduces the fundamental concepts and technologies used in low-power design verification with successful applications, best practices, and future trends shaping the industry. Through this, the study will demonstrate how the performance and efficiency of semiconductor devices can be improved, and they can become socially beneficial, too.

2. Semiconductor Design Verification Process

Semiconductor design verification is a critical process that verifies that semiconductor designs work as expected, how long they will work, and that they are reliable. The principal is to prevent design errors, inefficiencies, and failures that may happen through manufacturing. Verification is the most important part of checking that the design performs as per the desired values across conditions and abides by performance targets and budget power consumption (Mahmood et al., 2024). As in the cases of low-power designs, verification is also used to validate any potential issues affecting device performance, including power leakage, signal integrity failure, or thermal issues.

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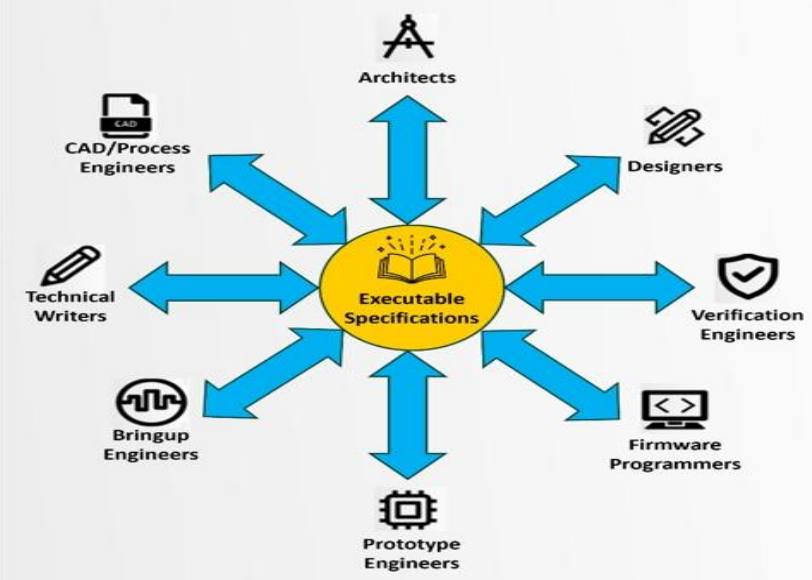

Figure 1: Specification automation

2.1 Defining Semiconductor Design Verification

The semiconductor design verification process involves checking that the semiconductor design performs well and meets the specified functional and non-functional requirements. This process goes through various design flow stages before and after silicon verification to ensure the design is correct (functionally) and optimal (in terms of power, speed, and thermal characteristics). Verification in such low-power semiconductor architectures becomes even more critical. It is no longer the case that power consumption is treated as a secondary and secondary design objective. It is a primary design objective. Verification for low power is met by verifying the design for energy efficiency across a wide spectrum of operating conditions and confirming that the design adheres to pre-defined power budgets. Pergament features such as dynamic voltage and frequency scaling (DVFS), clock gating, and power gating are verified to ensure the plantation is correct (Antonio et al., 2017). Through verification, engineers can confirm that the final silicon is functioning and best performing in terms of energy, with as little wasted energy as possible. The combination of simulation, emulation, and formal verification techniques is used to verify all of the designs to confirm that they satisfy their power constraints and functional requirements. A design may be prone to problems, such as consuming excessive power or generating high temperatures that might later be fixed using costly and time-consuming post-production.

2.2 Verification Tools for Low-Power Designs

Low-power designs are verified with a set of specialized tools that provide power-aware simulation and analysis accounts. Since power consumption analysis must address these complexities, these tools are necessary to validate low-power semiconductor architectures. Cadence, Synopsys, and Mentor Graphics are the three commonly used design verification tools. Cadence offers a great suite of verification tools (the tools range from power analysis to simulation). A tool for identifying power issues in a design, such as power consumption, voltage drop, and noise, which can affect the performance of low-power chips, is Cadence's Voltas, a power integrity analysis tool. The detailed insights into how power is consumed across disparate components of the chip that Voltas offers to designers give designers a basis for optimizing the design for energy efficiency. Synopsys also provides its Primetime PX solutions as part of the low-power verification offering. This tool is developed for low-power static timing analysis (STA) to analyze and optimize power consumption while satisfying all timing requirements. It combines power analysis and timer checking to ensure the design meets performance and power consumption goals. Synopsys' Design Compiler also offers power-aware synthesis to reduce power during the design synthesis phase.

Mentor Graphics, now part of Siemens, offers tools like PowerPro for power-aware design optimization. PowerPro is a power optimization and analysis tool that finds power hot spots in the design and thus lowers overall power consumption (Çakmak, 2024). The design is also integrated with other tools, including Calibre for physical design verification, to optimize it for high performance and low power operation. These verification tools can provide

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power usage details at various stages during the design process. Power analysis performed during simulation will identify power inefficiencies so that optimization can be done early on. These tools also integrate with other verification methods, including functional verification and formal verification, to assure all-around verification of the design.

Table 1: ***Verification Tools for Low-Power Designs***

Tool Provider	Tool Name	Purpose	Key Features
Cadence	Voltas	Power integrity analysis	Identifies power consumption, voltage drop, and noise
Synopsys	Primetime PX	Low-power static timing analysis	Combines power analysis and timing checks
Synopsys	Design Compiler	Power-aware synthesis	Optimizes power during synthesis
Mentor Graphics	PowerPro	Power optimization and analysis	Identifies power hotspots and optimizes energy usage

2.3 Integration of Design-for-Test (DFT) in Low-Power Designs

The Design for Test (DFT) methodology aims to make semiconductor designs testable and efficient for functional and non-functional concerns such as power consumption. Specifically, DFT techniques are crucial in low-power designs as they help find power inefficiency that can be missed. DFT embeds test structures and capabilities into the design to detect power problems during verification to more efficient designs. Scan chain insertion is a low-power design verification's most popular DFT technique. Scan cells are embedded within the design, making testing individual components easier (Zeltmann et al., 2016). The scan chains test the design in different functional behavior and power consumption perspectives. In low-power designs, scan chains can be set up to run tests to determine the power usage under varying modes, such as active, idle, and sleep, to ensure that power-saving features function as intended.

The other DFT methodology used to increase the testability of low-power designs is the built-in self-test (BIST). BIST allows the design to self-test during operation, thus eliminating the need for external test equipment. Since low-power design requires that its features operate with low power consumption while not dependent on a large power supply, BIST can test power management features like clock gating and power gating to verify that they function as intended without excessive power usage. Low-power designs are also integrated with boundary scan, a common DFT method to feature efficient testing of the connections between different components. Boundary scan assists in detecting the faults caused by the open or short in the power integrity, which can result in power inefficiencies. Integrating DFT in the low-power verification methodology detects power-related issues early in the design cycle with more reliable and energy-efficient semiconductor devices and associated devices (Aiden & Leonard, 2024). These methodologies increase the design's testability and optimize power consumption for the final product.

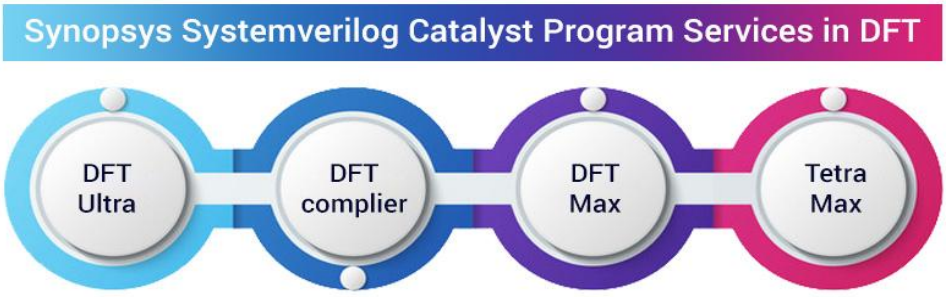

Figure 2: 5-solutions-for-optimal-dft-design-for-testability-in-lower-technology-nodes

3. Understanding Design-for-Test (DFT) in Low-Power Design

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3.1 What is Design-for-Test (DFT)?

Design for Test (DFT) is a set of techniques integrated into a semiconductor design process for making an end product testable regarding functionality, performance, and reliability. DFT is a concept where testability is achieved by directly incorporating it into the design of semiconductor devices for easy fault detection during the testing phase. It is necessary to this approach for semiconductor device functionalization and energy efficiency in low-power designs where low power consumption is of crucial priority. Modern semiconductor designs require a higher degree of testing to ensure reliability, and DFT techniques are particularly valuable as these designs keep becoming more complex. DFT allows testing various components on silicon chips, such as logic circuits, memory elements, and power management units, by embedding appropriate test structures and mechanisms into the chip's design (Koenemann, 2018). For these exact reasons, it is critical to ensure that low-power semiconductor devices, especially high-performance computing, graphics, and even AI accelerators, can deliver performance as required by state-of-the-art technologies (Konneru, 2021).

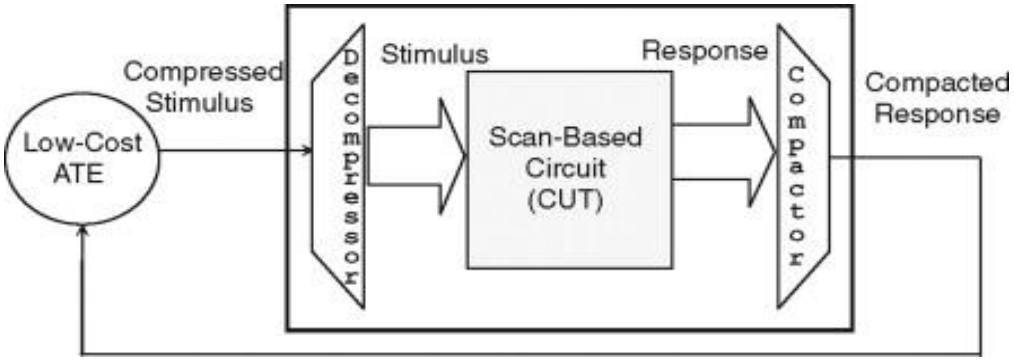

Figure 3: Test Compression

3.2 Benefits of DFT in Low-Power Design Verification

DFT is crucial for making low-power semiconductor devices reliable and efficient. Its most notable advantage is that it provides the capacity to enable power-efficient design validation at the expense of no loss in the test coverage required to verify its performance. Engineers can test various semiconductor components to report a device's power consumption, functionality, and performance, such that the device operates as specified within specified energy parameters using DFT (Jain et al., 2016). DFT techniques are used for low power design verification, where power consumption has to be kept minimal while the system functionality is not compromised beyond any level. DFT allows engineers to conduct power-aware simulations for different component performances under varying conditions by embedding testability into the design. Optimization of power-saving features and test existence is crucial to meet the power consumption requirement (Singh, 2022). DFT mitigates the risk of manufacturing defects leading to inefficiencies with the low power features of the device to operate as intended on the first silicon run. This helps achieve first-time silicon production and removes the need for costly rework or redesigns.

3.3 Key DFT Techniques for Low-Power Design Verification

Specifically, designed DFT techniques increase the testability of semiconductor low-power devices. Three widely used DFT techniques for VLSI low-power design are scan insertion, built-in self-test (BIST), and boundary scan, which enable the functional and power consumption requirements to be guaranteed.

Scan Insertion

Scan insertion is a very commonly used DFT technique that requires extra testing circuitry to locate faults within the chip's digital logic, making fault detection easier. This method creates a scan chain in which the circuit's internal nodes can be tested more efficiently (Wang et al., 2017). Because scan insertion helps the designers optimize power consumption for testing, it is beneficial for low-power designs. It helps solve the problem of locating faults that may lead to excessive energy usage and correcting them early in the design process.

Built-In Self-Test (BIST)

Another important DFT technique is the built-in self-test (BIST) in low-power design verification. BIST integrates self-testing in the semiconductor device, performing internal testing at design time and during manufacturing stages. This reduced redundancy of external equipment accessed for test purposes reduces power

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consumption during the verification because they usually have additional power consumption when used (Gill, 2016). BIST allows a device to execute internal self-tests to verify that the low-power features of the device are operating correctly. In addition, continuous self-testing also allows the detection of faults that may influence power consumption and maintain energy efficiency over the operational lifecycle.

Boundary Scan

The boundary scan technique implies testing interconnection between components on a semiconductor device. For easier access to internal signals during testing, it is necessary to place scan cells at the boundaries of the chip. Low-power designs are especially useful for boundary scans since engineers can verify that all parts are properly connected and that the power distribution scheme functions correctly. A boundary scan, in the case of multi-chip devices, guarantees that the whole system is tested for both performance and power efficiency, thus reducing the risk of power-inefficient devices due to faulty connections or signal routing. To design and verify low-power semiconductor designs, it is necessary to incorporate these DFT techniques, Scan insertion, BIST, and Boundary scan, into the design and verification process (Naveen Balaji & Chenthur Pandian, 2019). These methods guarantee that the devices operate within the energy constraints and increase the overall design reliability and functions. Embedding DFT within the semiconductor development process reduces first-time-right silicon production, decreases energy waste, and confirms device operation for real-world use.

Table 2: ***Key DFT Techniques for Low-Power Design Verification***

DFT Technique	Purpose	Key Benefits
Scan Insertion	Fault detection in chip's digital logic	Optimizes power consumption during testing
Built-In Self-Test (BIST)	Self-testing capability for the device	Verifies power management features like clock and power gating without external equipment
Boundary Scan	Testing interconnections between components	Ensures correct power distribution and fault detection in connections

4. GPU Hardware Validation for Low-Power Semiconductors

4.1 Introduction to GPU Hardware Validation

GPU hardware validation is a critical design step in the semiconductor design process, for example, for HPC systems and AI accelerators. Since GPUs are at the core of computationally demanding tasks, such as machine learning, scientific simulations, and real-time rendering, their proper function efficiency and power management are paramount. Validation ensures the hardware achieves the desired power consumption when indicating different conditions. This goes beyond simply verifying that the hardware works to validating the entire system to confirm operation with the necessary energy limits at the required power levels (Casolino et al., 2018). This is especially important given that modern GPUs consume power, and power consumption is a very important concern in modern GPUs for mobile and data center applications where thermal management and energy efficiency are becoming very important.

Techniques and methodologies for validating the GPU hardware for low-power operation must be there, with each technique and methodology dedicated to validating power inefficiencies and performance bottlenecks. The traditional way of validation has been to make sure that a chip or system meets its functions. For low-power applications, GPU validation suddenly broadens to whether the device manages its power at peak workloads, idle states, and under varying thermal conditions. As a result, this necessitates special techniques and simulation tools for GPU hardware validation of low-power semiconductor components, which simultaneously consider both performance and power consumption to achieve a more overall view of viable design in actual-world conditions.

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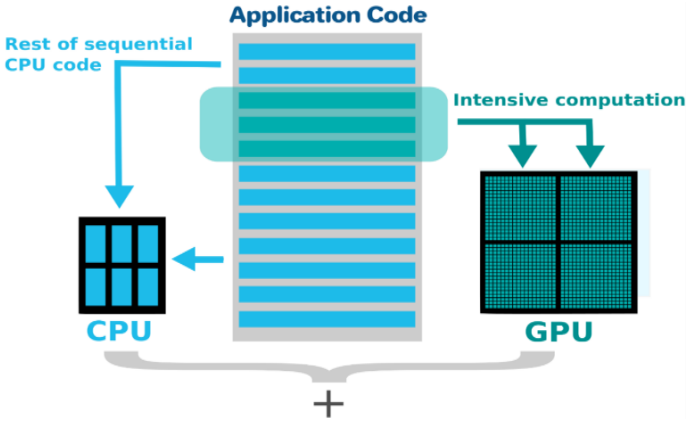

*Figure 4: **A guide covering how a GPU works***

4.2 Role of GPUs in High-Performance Computing and AI Accelerators

Modern devices using high-performance computing (HPC) systems and AI accelerators rely on GPUs to accomplish their work with massive parallelism loads. In contrast to early CPUs, which are great at sequential tasks, GPUs are especially good at parallel processors, allowing them to execute computation tasks efficiently in machine learning inference, video rendering, scientific simulations, and AI model training. Since GPUs can handle thousands of tasks at the same time, they are vital in areas where there is a necessity for a colossal amount of computational power (Chavan, 2021). GPUs are commonly used to perform heavy computational resources, such as running deep learning algorithms and artificial intelligence models, in the context of AI accelerator design. This use of resources is not sustainable in that they are used to the maximum. This is the case for data centers where their GPUs are employed for a long time or power consumption. Therefore, the power consumption of GPUs is not only to be optimized concerning their useable capabilities but also to be kept within reasonable values. For example, it is important to optimize power efficiency to reduce operation costs, prolong battery life, and prevent overheating in applications like autonomous drives and data centers.

Energy management plays a critical role in designing and operating GPUs used in HPC and AI and, therefore, has emerged as a key factor. The architectural improvements in the GPUs employ dynamic voltage and frequency scaling (DVFS), making them power efficient and changing their power consumption based on workload demands (Mishra & Khare, 2015). Moreover, with growing interest in reducing power consumption on such systems, GPU architecture is increasingly endowed with strategies such as energy-aware scheduling and workload optimization to achieve optimal performance while consuming minimum power. The need for high-performance GPUs is growing, and managing the power consumption of these GPUs effectively is not just a technical challenge but has become a major driver for the feasibility and viability of modern computing systems (Karwa, 2024).

4.3 Validating GPU Power Efficiency in Design Verification

GPU designs have become increasingly complex, making it hard to validate the power efficiency of GPUs in semiconductor design verification, specifically because GPUs must handle a wide range of workloads. Power validation is the process of using the GPU under various conditions. The GPU must meet the predefined energy consumption target and achieve the necessary performance levels. In particular, one of the main difficulties in this validation process is accurately measuring power consumption for all the real working environments, which have variable workloads. Several power analysis tools address this during the GPU design verification process. They enable the simulation of power consumption under various usage scenarios and indicate where optimizations can be made. To measure how much power computation draws at various points in its progress, techniques like hardware-based component power monitoring and software-based profiling are used to find inefficiencies. Engineers then analyze power usage at different levels of GPU architecture, such as three cores, memory, and interconnects, to identify components that consume relatively enormous amounts of energy (Li et al., 2016). It also adds power gating and clock gating techniques, limiting the GPU from consuming power if it is idle.

Simultaneously, the lack of necessary fission cross-section experiment data makes validating GPU power efficiency challenging. GPUs can do many diverse tasks, and their power consumption waxes and wanes with different forms of computation, number of active cores, and memory access patterns. For example, matrix multiplication in

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deep learning tasks can bring a significant direct proportion of the computation cores and memory subsystem to power consumption. For this reason, power efficiency should be validated under such workloads, introducing a combination of test scenarios, including peak load and idling conditions that are real-world applications. In addition, emulation and simulation environments modeling real-world workloads are some of the key solutions to GPU power validation. Engineers can then try the GPU design by running simulations of different workloads, such as AI, video rendering, or scientific simulations. Thermal dissipation is analyzed, and the GPU works within safe thermal limits to prevent overheating and extend reliability.

Power-efficient GPU designs generally include low-power states, which are enabled when the GPU is not under heavy load. For instance, if the GPU is idling, it may use lower power states, or if less demanding tasks run, clock speeds will be decreased. These low-power states are validated by checking GPU responsiveness to load changes, which can go into and out of the high and low-power modes without impacting performance. This validation allows for checking whether the GPU works efficiently under heavy load and conserving idle power for overall system energy efficiency. Validating GPU power efficiency is important in enabling low-power semiconductor design (Amelia, 2024). GPU hardware validation solves the problems of power monitoring, workload variability, and low-power state management to guarantee that GPUs will be capable of the demands of modern high-performance computing and AI applications while consuming a minimal amount of energy. This is necessary for performance and power efficiency to achieve the highest performance without zenithal energy overhead.

Table 3: ***Comparison of GPU Power Management Techniques***

Power Management Technique	**Purpose**	**Key Benefits**
Dynamic Voltage and Frequency Scaling (DVFS)	Adjusts voltage and frequency based on workload	Optimizes power consumption during peak workloads and idle states
Power Gating	Turns off power to inactive units	Reduces power consumption when certain components are not needed
Clock Gating	Disables clocks for idle components	Saves energy by reducing unnecessary clock activity

5. Ensuring First-Time-Right Silicon in Low-Power Design

5.1 Definition of First-Time-Right Silicon

The term first-time-right silicon means the successful fabricating of a semiconductor chip satisfying all design specifications such as performance, power efficiency, and functionality in the first run and to be held. For low-power applications, getting the first-time right silicon is very important as it will reduce the time and cost incurred by redesigning and re-fabricating. By eliminating first-time-right errors during the development process, first-time-right silicon can assume that the chip will perform as intended and be optimized for energy efficiency from the beginning. The highly competitive semiconductor industry must deliver products faster to meet customer demands for energy efficiency and performance by getting the design right the first time, with minimum effort and time lag. As semiconductor designs become more complex, achieving the first-time-right silicon has become increasingly important. It is a fine performance versus power consumption balance for high-performance computing systems, GPUs, and AI accelerators. The first attempt must be successful according to the above criteria. The design phase may take extra time and money to rectify and might have to return to the design stage. In addition, material cost and the environmental cost of wasted resources increase due to many silicon fabrication iterations (Dias et al., 2022). Furthermore, the right silicon eliminates costs for the first time and fits the increased demand for sustainable manufacturing practices.

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Figure 5: First Time Quality (FTQ)

5.2 Challenges in Achieving First-Time-Right Silicon

However, achieving first-time silicon is difficult, especially for low-power designs. Complex modern semiconductor architectures are one of the main problems engineer's faces. GPUs and AI accelerator designs need to achieve a balance of many such parameters like clock speed, processing power, memory usage, and, most importantly, power consumption. These factors need to be optimized simultaneously to operate the chip at the highest performance while meeting power constraints. Changing these parameters also makes it difficult to predict the exact results achieved from any given change, which increases the chances of mistakes. The power management problem in low-power designs increases complexity. Techniques such as dynamic voltage frequency scaling (DVFS) and power gating are needed to ensure that a chip can run energy efficiently without hurting its performance (Liu & Karanth, 2021). These techniques are complex and must be thoroughly tested under different conditions to prove that they reduce energy consumption to a minimum level. To predict how the design will behave for real-world applications, engineers are simulating a wide range of operating conditions, resulting in longer verification timelines.

Another problem comes in relying on simulation tools and techniques. Simulation is an indispensable step to ensure that a design will behave as expected, but it is not always predictive of real-world conditions. Uncertainties affect the silicon fabrication process due to variations in the manufacturing environment, the material properties of the chip, and the high architecture interaction properties. These factors may not be fully captured in simulations, and there may be discrepancies between the expected and actual chip performance. The correct design will require much testing and iterative refinement, which can bring the time to market.

Table 4: ***First-Time-Right Silicon Challenges***

Challenge	Description	Impact on Low-Power Designs
Complex Modern Architectures	Optimizing multiple parameters simultaneously	Increased difficulty in balancing performance and power consumption
Simulation Tools and Techniques	Discrepancies between simulation predictions and actual performance	Increases likelihood of errors in real-world chip behavior
Power Management Issues (e.g., DVFS)	Ensuring efficient power management under varying conditions	Requires thorough testing to ensure power savings without performance loss

5.3 Techniques for Achieving First-Time-Right Silicon in Low-Power Designs

Engineers have adopted many techniques for both design and verification processes that help overcome first-time-right silicon challenges. Early-stage simulation is one of the most important techniques. In early simulation, mind-boggling tools simulate and predict the design's behavior before it is physically fabricated. By running these simulations, the engineers can see potential problems with power consumption, performance, and functionality and make alterations at the beginning of the design phase. Cadence and Synopsys offer a complete simulation environment to analyze power consumption and performance in various conditions. Therefore, predictive analytics

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and simulation techniques used in the methodology of semiconductor development are vital to improving the efficiency of the design process in order to satisfy power and performance criteria without reworking. Design for Test (DFT) methodologies are another key technique to ensure that Entormakesilicon meets its power efficiency target. DFT is a practice that involves the incorporation of testability in design at the beginning, so it is easier to detect faults and inefficiencies at testing time. This is especially important since the interaction of multiple power management features must be more thoroughly verified in low-power designs. Engineers can use built-in self-test (BIST) and scan chain integration to validate each design component and verify that silicon yields the expected result. It eliminates the chance of error that otherwise would result in power inefficiencies or functional failure with the design process.

Extensive testing also ensures the first-time-right silicon. The design is then simulated, and physical testing, such as hardware validation, is performed to ensure the chip's physical operation as per expectations in real-world running conditions. In this context, it is very important to use real-world data when testing the chip so that its power management systems can work for real use cases. Furthermore, the chip is designed to be energy efficient across its operational lifecycle using additional power analysis techniques such as dynamic and static power analysis.

It is necessary to ensure collaboration among various engineering teams to attain the right silicon the first time. Therefore, design engineers, test engineers, and power specialists should collaborate so the design meets the performance requirements and the power consumption constraints. This optimizes all design aspects for energy efficiency and performance. It helps find potential issues early, and all members are part of that. If semiconductor engineers use these techniques, such as early-stage simulation, DFT, and extensive testing, to design low-power designs, the probability of the first-time-right silicon will increase (Chakravarthi, 2020). With the help of these advanced tools and methodologies, efficient, energy-conscious designs will be made for high-performance computing and AI accelerator applications.

6. Testing for Power Efficiency in Semiconductor Architectures

With advances in modern devices like mobile phones, wearables, and data centers, falling power efficiency is one of the most critical design parameters in semiconductor architecture. This increase in performance demand is especially for high-performance computing, graphics processing, and artificial intelligence (AI) accelerators. So, more designs are needed with high computational power and low energy consumption. Energy efficiency for data centers or mobile devices is vital to saving operational costs (Rong et al., 2016). Industries such as fleet management that use telematics emphasize power efficiency as part of their operating sustainability. Therefore, to successfully implement modern semiconductor technologies, the design of energy-efficient chips has ceased to be just a performance requirement and has become an integral part of the story.

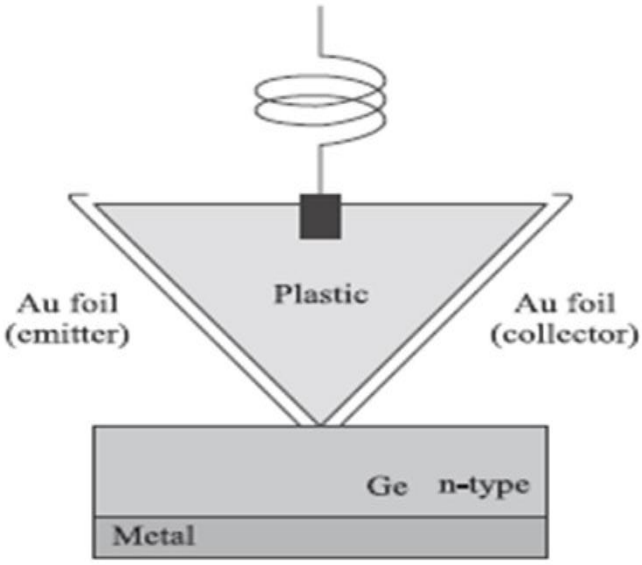

Figure 6: Exploring the Frontier of Semiconductor Technologies

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6.1 Power Consumption in Semiconductor Design

Power consumption, performance, and functionality are becoming the most important constructs in semiconductor design. As the capabilities of processors become more powerful, there becomes electrical energy consumption, increasing the difficulty of designing chips that achieve the speed at which they are needed without compromising their power efficiency. For example, power efficiency is of great importance not only for the longevity of the devices but also for cost reduction in the data centers as computing systems evolve into mobile devices, wearables, and cloud-based systems, resulting in computational systems, especially in AI-driven applications, which require real-time data processing, power management is very important. For GPUs and other AI accelerators that are above all the power-hungry components in high-performance computing systems, efficient designs have to minimize energy usage while providing a high enough performance (Vaithianathan et al., 2023). Power consumption in high-performance computing systems such as AI model powering systems and large-scale graphics rendering has to be managed without sacrificing performance. This is particularly crucial for semiconductor devices in data centers, where power consumption efficiency translates to reducing operational costs. Even in less power-intensive fields such as asset tracking, managing energy consumption is still a key factor in increasing operational efficiency, as mentioned in his study of telematics. Equally balanced power consumption in semiconductor design is crucial to keeping the device effective and sustainable.

6.2 Methods for Power Consumption Testing

Several methods are used to test a semiconductor design's power consumption to determine whether it meets its power efficiency targets for different states of operations. The results of these methods provide valuable insights about potential places that can be optimized to ensure that the final product will satisfy the energy consumption constraint. Power-aware simulation is one of the most used techniques for power consumption evaluation during design. The next method involves including the power models in the simulation environment to predict how the semiconductor will act under different environments. Designers can try to identify the parts of the circuit where power is lost before actual implementation (physical) by simulating circuit behavior (Kumar, 2019). It provides predictions of power-hungry components so that they can be identified early, reducing the probability of having to design the newly identified power-hungry component. Dynamic power analysis analyzes power consumption in the active mode during chip running tasks or executing instructions. This power consumption method concerns transistor switching activity and circuit states while processing power. The dynamic analysis also gives engineers an idea of the power consumption when the chip is under peak loads—an accurate depiction of how the chip will respond to real-world use.

Static power analysis looks at the device's power consumption when it is at a low power level or when the device is at rest. Such analysis is critical to make the chip use as little energy as possible when not performing data processing. Static power analysis can identify leakage currents that can cause power loss even if the device is in standby mode. To understand how energy can be efficiently maintained, such analyses are needed in the designs that must operate continuously using either minimal amounts of energy or none at all, as in IoT devices or wearable technologies (Nyati, 2018). However, each of these testing methodologies offers other ways for engineers to assess power consumption from different viewpoints so that it may be optimized for performing as actively as possible yet also economically.

Table 5: ***Techniques for Power Efficiency Testing***

Test Method	Focus Area	Key Features
Power-Aware Simulation	Simulates power consumption scenarios	Predicts power-hungry components, helps optimize the design
Dynamic Power Analysis	Power consumption during chip activity	Monitors power consumption under peak loads
Static Power Analysis	Power consumption during idle states	Identifies leakage currents during rest or standby modes

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6.3 Role of Testbench Creation in Low-Power Design Verification

Creating detailed test benches is crucial in testing power efficiency in semiconductor designs. More importantly, the testbench feeding into the core is a simulation environment that exercises the testbench and the core and checks functionality under various operational conditions, such as power consumption. These can be helpful in low-power design verification because the engineers can model the device's behavior over a wide variety of cases – like processing data or even during power state transitions. Test benches simulate a device's active and idle states to get a complete view of its power profile. A power-aware testbench measures the chip's power usage in real-time, allowing designers to identify inefficiencies that may or may not arise due to specific workloads or conditions (Bambagini et al., 2016). The test benches are used according to A, particularly useful in modeling corner cases in which a device may be subjected to extreme or unusual conditions. One of the essential corner cases is ensuring a good low-power design under all circumstances.

The test benches thus created can highlight power-related issues early enough to solve them before physical prototypes are realized. This decreases the risk of having to change or redesign the design once it is finalized. Test benches are used as notes to supplement the accuracy and efficiency of power testing during the design cycle process by predicting capabilities. There is a need to test the power efficiency in semiconductor architectures to guarantee that modern devices can operate within power boundaries while attaining optimum performance. The rapidly growing importance of power-efficient designs is due to using these with mobile devices, data centers, and high-performance computing systems. Key methodologies for power consumption simulation include power-aware simulation, dynamic power analysis, and power analysis, which are used at different design stages (Ouni et al., 2017). The detailed test benches also enhance verification of the power consumption so that low-power designs meet the standards for energy efficiency. These testing methodologies are necessary to achieve optimum performance of semiconductor devices at reduced environmental and operational costs.

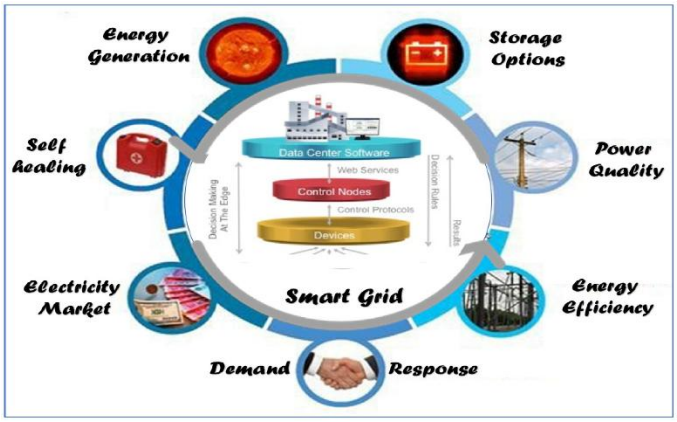

Figure 7: Smart electric grid.

7. Successful Case Study: Low-Power Design Verification in GPU Architectures

Table 6: ***Case Study: Low-Power Design Verification in GPU Architectures***

Design Challenge	Solution Implemented	Outcome
Power consumption of traditional GPUs	Integrated DVFS and DFT methods to optimize power usage	Achieved 30% reduction in power consumption while maintaining performance
High-performance workloads in GPUs	Used dynamic scaling to adjust power during peak workloads	GPU managed performance and power efficiently across all workloads
Design iteration and rework costs	Early detection of inefficiencies using DFT techniques	First-time silicon success, reducing time to market and rework costs

7.1 Introduction to the Case Study

The low-power GPU is important in the evolving semiconductor design, especially with the increased need for energy efficiency in high-performance computing and AI accelerators. Traditionally, GPUs are highly power-

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consuming, so reducing power wasted on lighting efficiency is vital. While this may be the case for some companies, as more companies look to create energy-efficient devices, companies also begin to explore ways to efficiently consume power without sacrificing performance. This case study determines how low-power design verification was successfully implemented in developing a next-generation GPU (Chen et al., 2016). The main focus was to reduce power consumption while the GPU could take on a high-performance workload, such as AI inference and 3D graphics rendering. An advanced design for test (DFT) and dynamic power management strategy were integrated to provide a power-efficient GPU architecture suitable for mobile devices and data centers. Due to the staggering challenge of balance in the design scale and financial constraints, the design team was able to meet both the performance and energy efficiency targets and was led into this path through the strategic use of power-aware verification.

7.2 Design Challenges and Solutions

Low-power GPUs include several inherent challenges. The most difficult obstacle is ensuring proper GPU performance during intensive computations like training a machine learning model or running graphics-heavy applications while maintaining low power consumption (Rodrigues, 2021). The power consumption of traditional GPUs, being tuned for raw performance, can be considerable and unacceptable in mobile devices and cloud environments. To solve these problems, the design team integrated dynamic voltage and frequency scaling (DVFS), a method of changing the voltage and frequency of the GPU components based on the working load. Using this method, the GPU will shed power to reduce consumption while still running at high performance during peak workloads. The GPU dynamically scales voltage and frequency to maintain good power efficiency across all operation states, maintaining good computational speed, which is critical for data center applications such as AI and HPC (Raju, 2017). Along with DVFS, the team also used DFT methods to test and verify the GPU's power consumption as a function of design and development. The DFT techniques, namely scan chains and built-in self-test (BIST), enabled comprehensive testing of individual components to confirm that the power management strategies were optimal and discover inefficiencies early at the design stage. By leveraging these methods, the team could narrow down where power consumption could be shrunk and tuned to meet energy efficiency goals. DFT use also provided a continuous feedback loop on the design, so the improvements in power efficiency were coherent with the performance target.

7.3 Achievements and Outcomes

Several interesting outcomes regarding the success of low-power design verification in this GPU architecture resulted. It also boasts a major decrease in overall power consumption. Compared to previous generations, the final design improves power usage by 30% using DVFS, which is key to mobile applications and energy-efficient data centers using the GPU's power management features. Without degrading performance, the dynamic power scaling succeeded in reducing this. Incorporating DFT techniques was essential to achieve the right silicon for the first time. They discovered power inefficiencies early in the design cycle, which precluded costly re-designs and enabled the final GPU to achieve performance and energy efficiency requirements on the first silicon run (Byna et al., 2022). This also meant that time to market was reduced, a critical factor in a very competitive semiconductor industry, and that the product could be delivered when promised and meet the strict power requirements that customers expect from a product.

The project resulted in better performance scalability and lower energy consumption. A wide range of workloads from low intensity to demanding computation processing was allowed to perform with high performance in the GPU. AI accelerators need robust performance for inference tasks and need to be energy efficient when idle, so what matters the most, in this case, is its efficient power management. The final design made this design more suitable for more applications, from high-end gaming to AI Processing to Edge Computing. The conclusion of the case study illustrates that modern GPU architectures should be developed with almost every low-power design verification technique integrated. The design team was able to faithfully create a GPU with high performance and low energy consumption by using DVFS, DFT, and power-aware simulation tools. One more time, the power-efficient design methods efficiency proves this result, and besides, the possibility of using such approaches in the semiconductor industry is forecasted to grow due to the growth of the energy-efficient demand in various sectors (Chavan & Romanov, 2023)

8. Best Practices for Ensuring Low-Power Design Verification

Low-power design verification in semiconductor architectures is a multi-dimensional process involving a lot of prescience and best practices that must be followed. The objective is to design energy-efficient structures that

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satisfy the performance requirements with reduced power consumption. This section highlights important best practices for ensuring low-power design verification, including a complete verification strategy, early power analysis, simulation, and team collaboration. These practices are essential for achieving success in low-power semiconductor verification and ensuring the designs are efficient, reliable, and sustainable.

Table 7: Low-Power Design Verification Best Practices

Best Practice	Purpose	Benefits
Comprehensive Verification Strategy	Ensures power analysis and validation throughout the lifecycle	Prevents costly redesigns and ensures power efficiency
Early Power Analysis and Simulation	Identifies potential inefficiencies before production	Reduces costs and time by optimizing power management early
Cross-Functional Collaboration	Involves design engineers, power specialists, and verification teams	Ensures optimal design performance and energy efficiency

8.1 Adopting a Comprehensive Design Verification Strategy

Semiconductor architecture must be verified for power efficiency and functionality without compromise. This has to proceed beyond the testing for the functional correctness phase and have a powerful power analysis and validation phase throughout the design life cycle. A proper and comprehensive verification strategy should combine the power analysis with the functional analysis that checks that the designs will meet the required performance metrics at the cost of saving power. Integrating power constraints into the original verification process reduces the probability of the redesign at a later stage. Verification must be done in one stage, starting with pre-silicon simulation and continuing to post-silicon validation. Early-stage simulation and testing for power efficiency are necessary to guarantee that the design meets power consumption goals, as stated in. Also, the design-for-test (DFT) methodologies, which make it possible to build test structures and checkpoints into the design, facilitate the continuous monitoring and optimization of the design's power performance during the process (Meixner & Gullo, 2021).

It includes a complete strategy that tests the design under different operating conditions to ensure the power efficiency remains the same under different workloads. It includes checking out the performance of the design under peak load, in idle states, and during power mode transitions. A proper verification strategy should consider the varying power requirements that different components and stages of the device are exposed to in normal operation. Since the semiconductor device is functional and power dependent, designers can systematically verify the device's functional and energy characteristics to guarantee its optimum performance and energy efficiency, which meets the specified standard.

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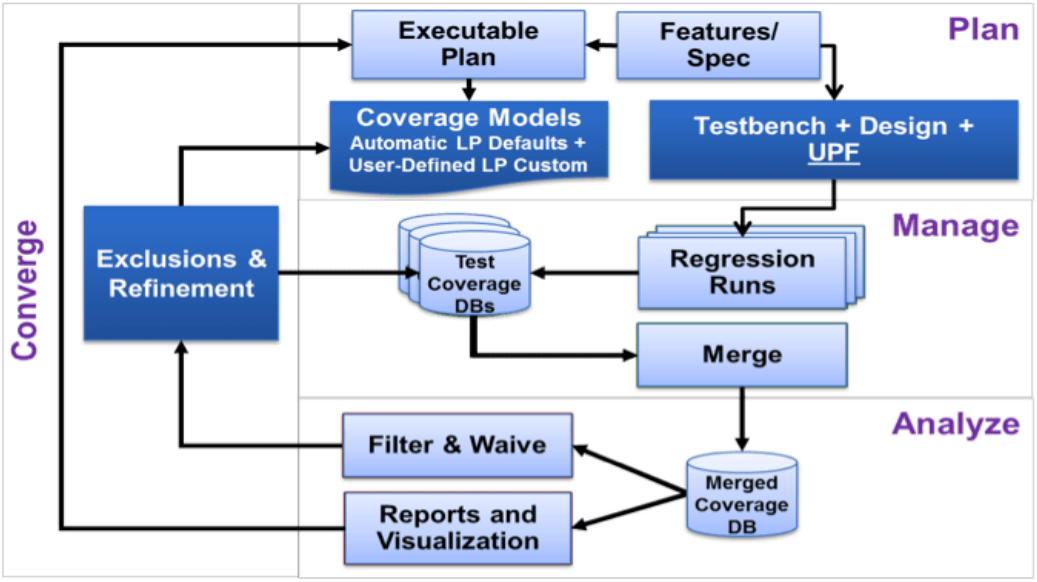

Figure 8: ***Coverage-Driven Verification Isn't Complete Without Low-Power Metrics***

8.2 Early Power Analysis and Simulation

Early power analysis and simulation are essential to identifying the source of power inefficiency before the initial design phase. Early opportunities for power analysis let design teams make educated decisions and continue with design while avoiding costly hardware production. (Dhaanagari, 2024) states that power analysis at the pre-silicon stage will provide power consumption hotspots, such as Circuits consuming more than expected power. By detecting this early, engineers get a valuable 2 to 3 weeks to make adjustments to the design, optimize the circuitry, or include power management features. Early power analysis would not be possible without simulation tools since they permit power consumption scenarios to be tested on the chip level without spending time and money building physical prototypes. Depending on the allocation of the simulation, it can predict the power consumption of different components in a given design and identify locations that benefit from employing energy-saving techniques. Common powers estimation tools like Synopsys's Primetime and Cadence's Voltus are used to study how power will behave across the design, and engineers can get insights into how the power will behave with these tools. With an early application of simulation tools to model the whole system, engineers eliminate the possibility that problems become expensive problems later.

Emerging low-power semiconductor architectures further complicate the issue of power analysis, demanding early-stage power analysis, which is critical to help ensure energy efficiency. The resulting design satisfies functional and power consumption goals through this process. These early checks make it much easier to remedy power problems down the line, and delays are greatly minimized from the costs incurred. Early power simulations and assessments using notes are important to achieve scalable, energy-efficient designs (Sardana, 2022).

8.3 Collaboration across Teams for Successful Low-Power Designs

Another best practice of successful low-power design verification is to generate effective collaboration between design engineers, verification teams, and power specialists where needed. In practice, power design verification is a complex, multi-team, multi-disciplinary process that requires input from multiple teams with different specializations and skill areas. The success of low-power designs depends largely on face-to-face collaboration between the engineers in charge of different aspects of the design, functionality, power optimization, and verification. It is the responsibility of design engineers to develop the semiconductor device by building its architecture and components. However, to meet power efficiency goals, the designs need to leverage input from power specialists for strategies like dynamic voltage and frequency scaling (DVFS) or power gating. On the other hand, verification teams ensure the design does what it should. It does not exceed the power consumption limits. These teams can work together from the beginning when the design phase starts and make the best design for solving any potential issue early on.

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Cross-functional collaboration also helps integrate DFT methodologies that are important for testing low-power designs. The design engineers must work extremely closely with the verification team so that power analysis and testing are part of the design. By involving power specialists in design engineering, they can see how the architecture should be optimized for low power. The verification teams can also ensure the design has the power consumption that targets them, as power is crucial to electronic product development. Verifying low-power designs in semiconductor architectures should be accomplished with complete verification strategies, early power analysis, simulation, and seamless cross-team collaboration. By implementing these best practices, design teams can improve their power efficiency, reduce the chances of an expensive redesign, and enhance high performance in the increasingly evolving technological world.

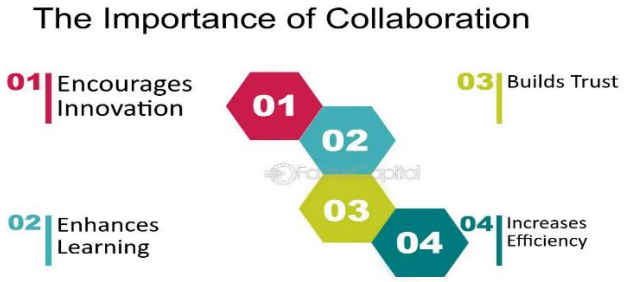

Figure 9: ***The Importance of Collaboration***

9. Future Trends in Low-Power Design Verification for Semiconductors

The semiconductor business is changing rapidly, and new advances in low-power design verification are coming quickly to market. This drives the need to evolve low-power verification tools and techniques in the face of increasing energy efficiency requirements in almost every application space, from mobile devices to data centers. The future of low-power design verification will be primarily driven by emerging technologies, automation, AI-driven tools, and, eventually, the promised power-saving potential of Quantum computing.

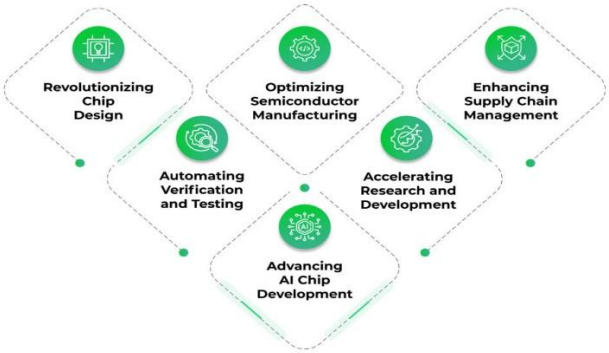

Figure 10: the-future-of-semiconductor-design-a-generative-ai-approach

9.1 The Evolution of Low-Power Verification Tools and Techniques

It is expected to significantly improve the low-power design and low-power functionality with the help of emerging technologies such as AI-diversification tools and machine learning. Traditional verification methods, such as simulation and emulation, consume a huge amount of hardware and time. AI-based tools can speed up the pattern recognition process, finding power inefficiencies and better optimizing design parameters faster than human engineers (Saad et al., 2024). Early verification of power leakage issues by AI-driven tools helps engineers estimate potential leakage problems in the earlier design phase. It thus reduces the requirement for reworks later in the process. Machin learning algorithms can process large amounts of design data to find the patterns that maternal probable energy efficiency or power consumption failures. This predictive capability can allow engineers to avoid potential errors that might otherwise entail an expensive cost of design iteration. Also, using AI and machine learning can also incorporate real-world use case scenarios to improve power consumption models for better energy

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consumption simulations. AI-driven verification tools will get smarter, and they will be able to handle more complicated semiconductor designs, retaining energy efficiency with an increase in optimal performance (Singh, 2023). Automating repetitive tasks like checking for compliance with power constraints and other functional requirements will streamline the verification process and free engineering's hand to tackle more challenging problem-solving tasks. Eventually, this shortens the time and reduces the cost during the low-power design verification process, making it possible for companies to use energy-conscious solutions without sacrificing performance.

9.2 Integration of Quantum Computing and Semiconductor Design

Revolutionizing semiconductor architectures, including low-power ones, is a promising realm in quantum computing. The advantage of quantum computers is that they do their work with quantum bits (qubits) and cannot do some things that classical computers can. This advancement in low-power semiconductor designs would be a big win, specifically in high-performance computing (HPC) and AI systems. Quantum computing may have unique approaches to solving hard optimization problems in the context of low-power design verification (Gill et al., 2022). For example, quantum algorithms could more efficiently simulate less powerful semiconductor designs than classical methods without testing or simulation. In addition, quantum computers could also provide new methods for optimizing the power consumption of semiconductor devices by using techniques that find configurations that utilize less power. These methods are not readily apparent when using conventional methods. To verify circuits of interest to quantum systems, the verification processes for low-power semiconductor architectures must be evolved to account for the specialties of quantum systems. It could be to design new verification tools to simulate quantum behavior or to ensure that low-power quantum circuits meet energy efficiency requirements. Despite being in its early stages of fully integrating quantum computing into the semiconductor design, power efficiency's potential revolution is not to be ignored. Since quantum hardware will become more accessible, quantum computing will be adopted more by semiconductor verification, where the industry will move toward more efficient, low-power designs.

9.3 The Role of Automation and AI in the Future of Design Verification

Automated and AI-driven verification of the low-power design will be key enablers to the future of low-power design verification, as this will make the verification process fast and decrease its time and cost greatly to verify the energy-efficient semiconductor designs. Due to the complexity of modern semiconductor architectures, they are trying to address, supported by the waning of people to hand construct myriads of comprehension vector generators in order to guarantee the most effective run and speedup of their verification, it has turned out vital to deliver into the manually made software and hardware instrumentation a collection of automatically used instruments to assure verification procedure. Automated verification tools are based on extensive simulations that can run and check power constraints across the design iterations (Bindra & Mantooth, 2019). At an early stage, these tools can discover likely power inefficiencies, which can be fixed before the design enters costly phases. This can be further enhanced by AI-driven tools that learn from past design cycles and improve at deciding if a problem will occur.

AI can automate the optimization process of selecting low-power solutions based on given performance targets and energy consumption goals. For instance, AI can dynamically tune voltage and frequency scaling while living within real-time power consumption limits to get optimal performance. While these environments promise high power efficiency, this dynamic adaptation will become critical for dynamic adaptation (Goel & khramhabhatt, 2024). Using AI and automation in the verification process will accelerate the testing rate, decrease human error, and improve the reliability of designs with low power. These technologies will continue to mature, ensuring energy-efficient semiconductor devices are more efficient and enabling companies to satisfy this growing demand by creating low-power systems at lower costs and less time to develop.

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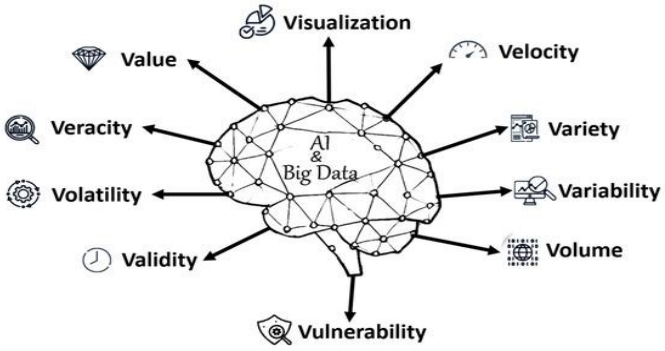

Figure 11: The spectrum of Vs.

10. Conclusion

With the growing digitization of our world and the associated requirement to increase the functionality of semiconductor devices, there is an explosive need for energy-efficient devices capable of powering graphs, high-performance computing, and AI accelerators. However, as more and more people drove to have faster, smaller, and more efficient devices, secondary designers slowly gathered Reid and more bot-taking devices. Critical integration of technologies such as Design for Test (DFT) and GPU hardware validation has occurred to meet these objectives throughout the design lifecycle. By power-aware simulation and using these special verification tools, this process identifies and mitigates potential power inefficiencies early in time before they need costly reengineering and, with the first time, the right silicon. Due to its significance in semiconductor architecture, low-power design verification is not merely a technical challenge. It is a reaction to global environmental and economic imperatives. In this light, optimizing the power consumption of devices from mobile phones to data centers has become a key point in reducing operation costs and increasing battery lifetime. Dynamic voltage and frequency scaling (DVFS), clock gating, and power gating constitute very effective techniques that can achieve energy efficiency without performance degradation. This design verification is necessary to ensure power-saving features work as expected within all operational conditions.

DFT methods like scan insertion, built-in self-test (BIST), and boundary scan play an essential role in making the low-power designs testable so that the engineers can check power inefficiencies and improve performance earlier in the design stage. With the combined use of these techniques together with the sophisticated power analysis tools provided by leading vendors such as Cadence, Synopsys, and Mentor Graphics, semiconductor designers have a mechanism to detect power hotspots and to correct the problem before physical prototypes are made, thereby saving both time and money in the design cycle. With the rise in the use of GPUs in AI and machine learning tasks, it has become essential to validate GPU hardware, particularly to improve GPU's power management. Power efficiency under different conditions is necessary for these modern GPUs because they are complex devices. It is not only about assessing the power consumption at the peak of the work and the GPU power consumption at low or idle states while transitioning to/from different power modes. Engineers can apply power-aware testbenches to simulate real-world scenarios and guarantee that GPUs satisfy performance and energy OR efficiency targets. Given the speed with which emerging technologies like AI, edge computing, and quantum computing are changing industries, the demand for especially low-power semiconductor architectures will remain the same. Further integration of tools driven by AI verification and machine learning is expected to speed up the process of power analysis and optimization tasks in low-power design verification via automation. These will enable shorter innovation cycles and lower energy-efficient design costs.

Quantum computing is integrated into semiconductor design, suggesting a very interesting frontier with the potential of altering how power consumption will be addressed in next-generation devices. Automation and AI have become essential in streamlining the verification process, and they will continue moving forward as the industry progresses and adopts AI and automation. Through this, designers will push the boundaries of what is achievable in low-power semiconductor design to follow up with the growing need for sustainable and highly performing devices. That semiconductor architecture cannot exist without low-power design verification. Using them, one can combine the power consumption requirements of high-performance applications with advanced verification techniques such as DFT and GPU validation. However, as the industry moves forward with innovation, the quest for the next

generation of energy-efficient semiconductor technologies will rely on the constant progression of verification methodologies, and its continuous advancements will steer energy-efficient development of more sustainable, power-efficient devices that will break the path for the computing future.

References;

[1] Aiden, L., & Leonard, Z. (2024). Low-Power Semiconductor Design: AI and UVM-Based Verification Strategies.

[2] Amelia, O. (2024). AI-Driven Testing and Validation Techniques for Low-Power Semiconductor Design Verification Using UVM.

[3] Antonio, R. A., de la Costa, R. M., Ison, A. R., Lim, W. K., Pajado, R. A., Roque, D. B., ... & Alarcon, L. (2017, November). Implementation of dynamic voltage frequency scaling on a processor for wireless sensing applications. In *TENCON 2017-2017 IEEE Region 10 Conference* (pp. 2955-2960). IEEE.

[4] Bambagini, M., Marinoni, M., Aydin, H., & Buttazzo, G. (2016). Energy-aware scheduling for real-time systems: A survey. *ACM Transactions on Embedded Computing Systems (TECS)*, *15*(1), 1-34.

[5] Bindra, A., & Mantooth, A. (2019). Modern tool limitations in design automation: Advancing automation in design tools is gathering momentum. *IEEE Power Electronics Magazine*, *6*(1), 28-33.

[6] Byna, S., Idreos, S., Jones, T., Mohror, K., Ross, R., & Rusu, F. (2022). *Position Papers for the ASCR Workshop on the Management and Storage of Scientific Data*. US Department of Energy (USDOE), Washington DC (United States). Office of Science.

[7] Çakmak, R. (2024). Design and implementation of a low-cost power logger device for specific demand profile analysis in demand-side management studies for smart grids. *Expert Systems with Applications*, *238*, 121888.

[8] Casolino, G. M., Russo, M., Varilone, P., & Pescosolido, D. (2018). Hardware-in-the-loop validation of energy management systems for microgrids: A short overview and a case study. *Energies*, *11*(11), 2978.

[9] Chakravarthi, V. S. (2020). *A practical approach to VLSI system on chip (SoC) design*. Springer International Publishing.

[10] Chavan, A. (2021). Eventual consistency vs. strong consistency: Making the right choice in microservices. International Journal of Software and Applications, 14(3), 45-56. https://ijsra.net/content/eventual-consistency-vs-strong-consistency-making-right-choice-microservices

[11] Chavan, A., & Romanov, Y. (2023). Managing scalability and cost in microservices architecture: Balancing infinite scalability with financial constraints. *Journal of Artificial Intelligence & Cloud Computing, 5*, E102. https://doi.org/10.47363/JMHC/2023(5)E102

[12] Chen, Y. T., Cong, J., Fang, Z., Lei, J., & Wei, P. (2016). When Spark Meets {FPGAs}: A Case Study for {Next-Generation}{DNA} Sequencing Acceleration. In *8th USENIX Workshop on Hot Topics in Cloud Computing (HotCloud 16)*.

[13] Dhanagari, M. R. (2024). Scaling with MongoDB: Solutions for handling big data in real-time. *Journal of Computer Science and Technology Studies, 6*(5), 246-264. https://doi.org/10.32996/jcsts.2024.6.5.20

[14] Dias, P. R., Schmidt, L., Chang, N. L., Lunardi, M. M., Deng, R., Trigger, B., ... & Veit, H. (2022). High yield, low cost, environmentally friendly process to recycle silicon solar panels: Technical, economic and environmental feasibility assessment. *Renewable and Sustainable Energy Reviews*, *169*, 112900.

[15] Gill, P. (2016). *Electrical power equipment maintenance and testing*. CRC press.

[16] Gill, S. S., Kumar, A., Singh, H., Singh, M., Kaur, K., Usman, M., & Buyya, R. (2022). Quantum computing: A taxonomy, systematic review and future directions. *Software: Practice and Experience*, *52*(1), 66-114.

[17] Goel, G., & Bhramhabhatt, R. (2024). Dual sourcing strategies. *International Journal of Science and Research Archive*, 13(2), 2155. https://doi.org/10.30574/ijsra.2024.13.2.2155

[18] Jain, A., Shin, Y., & Persson, K. A. (2016). Computational predictions of energy materials using density functional theory. *Nature Reviews Materials*, *1*(1), 1-13.

[19] Karwa, K. (2024). The role of AI in enhancing career advising and professional development in design education: Exploring AI-driven tools and platforms that personalize career advice for students in industrial and product design. *International Journal of Advanced Research in Engineering, Science, and Management*. https://www.ijaresm.com/uploaded_files/document_file/Kushal_KarwadmKk.pdf

[20] Koenemann, B. (2018). Design-for-test. In *EDA for IC System Design, Verification, and Testing* (pp. 21-1). CRC Press.

[21] Konneru, N. M. K. (2021). Integrating security into CI/CD pipelines: A DevSecOps approach with SAST, DAST, and SCA tools. *International Journal of Science and Research Archive*. Retrieved from https://ijsra.net/content/role-notification-scheduling-improving-patient

[22] Kumar, A. (2019). The convergence of predictive analytics in driving business intelligence and enhancing DevOps efficiency. International Journal of Computational Engineering and Management, 6(6), 118-142. Retrieved from https://ijcem.in/wp-content/uploads/THE-CONVERGENCE-OF-PREDICTIVE-ANALYTICS-IN-DRIVING-BUSINESS-INTELLIGENCE-AND-ENHANCING-DEVOPS-EFFICIENCY.pdf

[23] Li, D., Chen, X., Becchi, M., & Zong, Z. (2016, October). Evaluating the energy efficiency of deep convolutional neural networks on CPUs and GPUs. In *2016 IEEE international conferences on big data and cloud computing (BDCloud), social computing and networking (SocialCom), sustainable computing and communications (SustainCom)(BDCloud-SocialCom-SustainCom)* (pp. 477-484). IEEE.

[24] Liu, S., & Karanth, A. (2021, December). Dynamic voltage and frequency scaling to improve energy-efficiency of hardware accelerators. In *2021 IEEE 28th International Conference on High Performance Computing, Data, and Analytics (HiPC)* (pp. 232-241). IEEE.

[25] Mahmood, S., Sun, H., Ali Alhussan, A., Iqbal, A., & El-Kenawy, E. S. M. (2024). Active learning-based machine learning approach for enhancing environmental sustainability in green building energy consumption. *Scientific Reports*, *14*(1), 19894.

[26] Meixner, A., & Gullo, L. J. (2021). Design for Test and Testability. *Design for Maintainability*, 245-264.

[27] Mishra, A., & Khare, N. (2015). Analysis of DVFS techniques for improving the GPU energy efficiency. *Open Journal of Energy Efficiency*, *4*(4), 77-86.

[28] Naveen Balaji, G., & Chenthur Pandian, S. (2019). Design of test pattern generator (TPG) by an optimized low power design for testability (DFT) for scan BIST circuits using transmission gates. *Cluster Computing*, *22*, 15231-15244.

[29] Nyati, S. (2018). Transforming telematics in fleet management: Innovations in asset tracking, efficiency, and communication. International Journal of Science and Research (IJSR), 7(10), 1804-1810. Retrieved from https://www.ijsr.net/getabstract.php?paperid=SR24203184230

[30] Ouni, B., Mhedbi, I., Trabelsi, C., Atitallah, R. B., & Belleudy, C. (2017). Multi-level energy/power-aware design methodology for MPSoC. *Journal of Parallel and Distributed Computing*, *100*, 203-215.

[31] Raju, R. K. (2017). Dynamic memory inference network for natural language inference. International Journal of Science and Research (IJSR), 6(2). https://www.ijsr.net/archive/v6i2/SR24926091431.pdf

[32] Rodrigues, A. O. (2021). *A Framework for Mobile Augmented Reality in Urban Maintenance* (Master's thesis, Universidade NOVA de Lisboa (Portugal)).

[33] Rong, H., Zhang, H., Xiao, S., Li, C., & Hu, C. (2016). Optimizing energy consumption for data centers. *Renewable and Sustainable Energy Reviews*, *58*, 674-691.

[34] Saad, S., Haris, M., Ammad, S., & Rasheed, K. (2024). AI-assisted building design. In *AI in material science* (pp. 143-168). CRC Press.

[35] Sardana, J. (2022). Scalable systems for healthcare communication: A design perspective. *International Journal of Science and Research Archive*. https://doi.org/10.30574/ijsra.2022.7.2.0253

[36] Singh, V. (2022). EDGE AI: Deploying deep learning models on microcontrollers for biomedical applications: Implementing efficient AI models on devices like Arduino for real-time health monitoring. International Journal of Computer Engineering & Management. https://ijcem.in/wp-content/uploads/EDGE-AI-DEPLOYING-DEEP-LEARNING-MODELS-ON-MICROCONTROLLERS-FOR-BIOMEDICAL-APPLICATIONS-IMPLEMENTING-EFFICIENT-AI-MODELS-ON-DEVICES-LIKE-ARDUINO-FOR-REAL-TIME-HEALTH.pdf

[37] Singh, V. (2023). Federated learning for privacy-preserving medical data analysis: Applying federated learning to analyze sensitive health data without compromising patient privacy. International Journal of Advanced Engineering and Technology, 5(S4). https://romanpub.com/resources/Vol%205%20%2C%20No%20S4%20-%2026.pdf

Journal of Information Systems Engineering and Management
2025, 10(45s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

[38] Vaithianathan, M., Patil, M., Ng, S. F., & Udkar, S. (2023). Comparative study of FPGA and GPU for high-performance computing and AI. *ESP International Journal of Advancements in Computational Technology (ESP-IJACT)*, *1*(1), 37-46.

[39] Wang, X., Zhang, D., He, M., Su, D., & Tehranipoor, M. (2017). Secure scan and test using obfuscation throughout supply chain. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *37*(9), 1867-1880.

[40] Zeltmann, S. E., Gupta, N., Tsoutsos, N. G., Maniatakos, M., Rajendran, J., & Karri, R. (2016). Manufacturing and security challenges in 3D printing. *Jom*, *68*(7), 1872-1881.